TESTING WITH INTERNAL ACCESS

MASSIVE (TOTAL) OBSERVABILITY

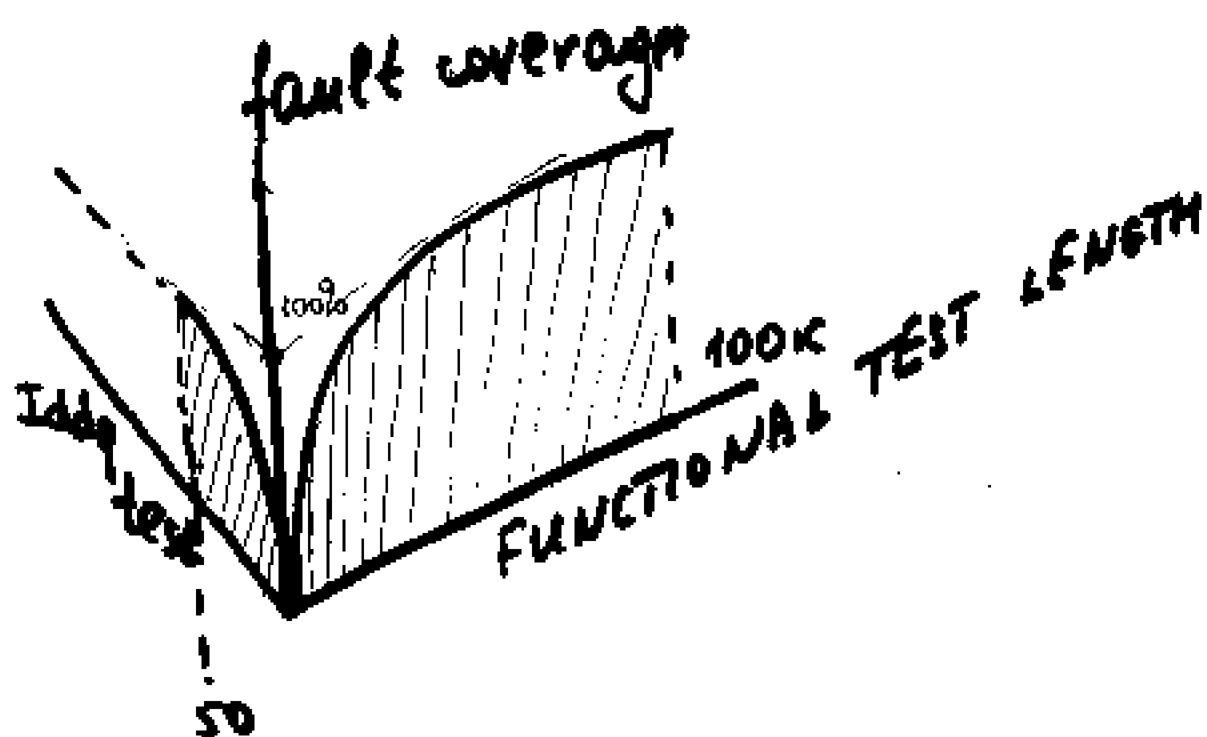
MEASURING THE quiescent POWER SUPPLY CURRENT

(IDDQ TESTING)

VERY POPULAR FOR STATIC CMOS TECHNOLOGY.

MOST STUCK-AT AND BRIDGING FAULTS RESULT IN A DRASTIC INCREASE IN THE POWER SUPPLY CURRENT.

• STATIC CURRENT DISSIPATING BLOCKS such as SENSE-AMPS, differential logic must be switched off during Iddq testing.



design for Iddqability ⟹ DUT should not have high current states

FOR CURRENT (Iddq) testing we do not need an assumtion that BFs result in AND or OR between lines which are bridged. (For voltage testing this assumption is required).

BFs are about 50%-60% of all faults

(Rajsuman, IDDQ TESTING FOR CMOS VLSI, ARTECH HOUSE, 1995)

BUILT-IN CURRENT TESTING (BIC) WAS presented in:

W. MALY, P. NIGH, "BUILT-IN CURRENT TESTING", Proc. IEEE CAD CONF. 1988 pp340-343

FOR CMOS when not actually switching one transistor in a CMOS pair is off so the circuit draws only a leakage current of about 100 pA, so the total leakage current for even large IC is few μAs. For faults this current is drastically grows.

Threshold: (1 ÷ 10) μA

. I_{DDQ} can identify "walking wounded" chips, which still produce correct outputs but already requiring more current consumption.

- In addition to leakage currents IDDQ currents for a fault-free network which contains a component which depends on input vectors (state dependent component)

- Estimation of IDDQ for a fault-free network is difficult (NP-complete) problem.

- Most people use upper bounds for a fault free IDDQ

- To compute these upper bounds one measure <u>currents for test patterns.</u>
  This approach is applied when the fault-free device is <u>partitioned</u> into blocks.
  Then the upper bound is the <u>sum of currents for all blocks</u>
- <u>Problem</u>: leakage currents are growing with the increasing size of a DUT.
- IDDQ should be used in combination with voltage testing

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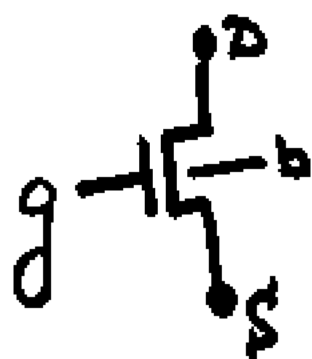
TRANSISTOR FAULTS



6 shorts for every transistor

(s g), (s, D), (s b)

(g, D), (g, b) (D, b)

MOST STUCK-AT AND SHORTS RESULT IN

A DRASTIC INCREASE IN a ~~pow~~ current consumption for some INPUTS

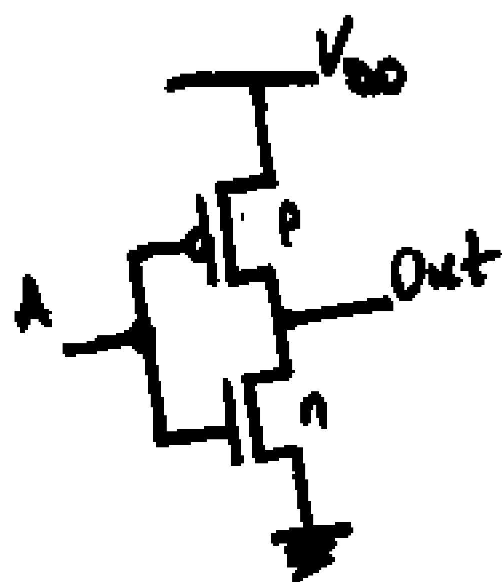
Detection of an <u>optimal threshold</u> for the current is an experimental iterative procedure.

- About 3% of ICs that pass all other test fail I_{DDQ}.

- About 8% of faults manifested themselves during 1,000 hours for 59,000 ICs, which passed all tests except I_{DDQ}

(Ford Microelectronics, 1995)

EXAMPLE INVERTER



(s,d) short for n transistor is detected when A=0; (Out/0)

(s,d) short for p transistor is detected for A=1 (OUT/1)

(Aitken, "A Comparison of Defect models..." Proc ITC, 1992 pp 778-787.;

GULATI, MAO, GOEL, "DETECTION OF "UNDECTABLE" FAULTS BY IDDQ" Proc. ITC, 1992 pp 770-777)

In many cases there are several levels of current consumtion for the faulty device depending on an input vector. This information ("current signature") provides for some diagnostic resolution

(W. MALY, Proc. VLSI Symp. PRINCETON, NJ. 1996)

IDDQ may be also used for failure analysis and design verification

- I DDQ TESTING IS SLOW!
- TYPICALLY LESS THAN 1,000 test patterns can be applied.
- PROBLEM OF GENERATION OF SHORT TESTS IS VERY IMPORTANT FOR IDDQ.

<u>GOAL</u>: DETECTION OF SINGLE STUCK-AT AND BRIDGING FAULTS

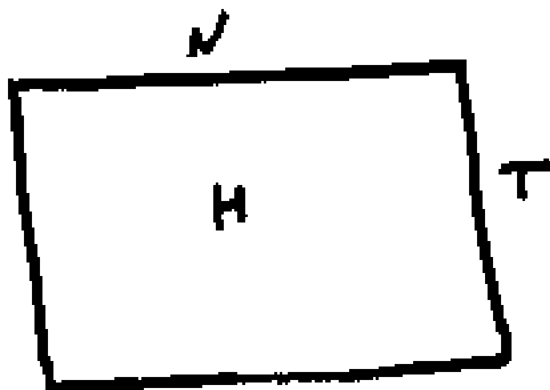
NUMBER OF FAULTS:

$$2N + \binom{N}{2} = \frac{1}{2}(N^2 + 3N)$$

where N is a number of nodes

TEST MATRICES H

FOR A NETWORK WITH N nodes rows OF H represent logical values at all nodes for a given test pattern.



T - number of test patterns.

T1 All BFs and SSFs are detectable iff all columns in a test matrix H are different and not equal to all zeros and all ones

Let: m - number of <u>input</u> nodes
p - number of <u>internal</u> nodes
n - number of <u>output</u> nodes

$N = m + p + n$

I2.

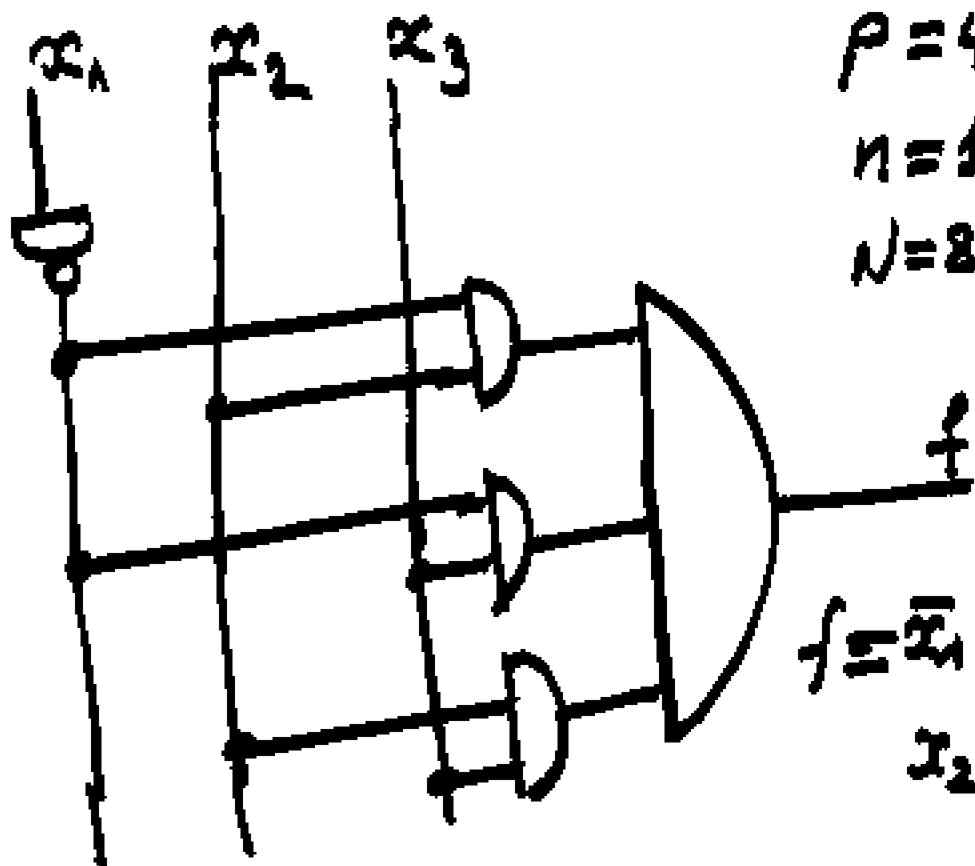
$$\lceil \log_2 (m+n+p+2) \rceil \le T \le \lceil \log_2 (m+2) \rceil + p + n$$

THE LOWER BOUND is ATTAINED FOR one NAND gate with N-1 inputs

THE UPPER BOUND is ATTAINED FOR TWO-LEVEL AND-OR NETWORKS WITH ORTHOGONAL PRODUCT TERMS

$$T \le N$$

EXAMPLE



$m=3$

$p=4$

$n=1$.

$N=8$

$$f=\bar{x}_1 x_2+\bar{x}_1 x_3+x_2 x_3$$

	x_1	x_2	x_3	$\bar{x}_1$	$\bar{x}_1 x_2$	$\bar{x}_1 x_3$	$x_2 x_3$	F
$H=$	1	1	1	0	0	0	1	1
	0	0	1	1	0	1	0	1
	0	1	0	1	1	0	1	1
	0	1	1	1	1	1	0	0
	0	0	0	1	0	0	0	0

$T=5$

All columns are different and contain 0's and 1's

TESTING OF TWO-LEVEL UNATE NETWORKS

AND-OR, NAND-NAND, NOR-NOR, OR-AND.

Let $f(x_1^*, x_2^*, \ldots, x_m^*)$ is unate $x_i^* \in \{x_i, \bar{x}_i\}$.

Let H_{IN} is matrix with rows being test patterns. Then columns of H_{IN} are

$$\underbrace{(11\ldots1\overset{i}{0}1\ldots11)}_{m+1}^{TR} \text{ if } x_i^* = x_i$$

$$\underbrace{(00\ldots0\overset{i}{1}0\ldots00)}_{m+1} \text{ if } x_i^* = \bar{x}_i$$

Example

$$f(x_1, x_2, x_3) = \overline{x_1}\, x_2 + \overline{x_1}\, x_3 + x_2 x_3$$

$$x_1^* = \overline{x_1}\ ,\ x_2^* = x_2\ ,\ x_3^* = x_3$$

$$K_{IN} = \begin{bmatrix} 1 & 1 & 1 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \end{bmatrix}$$

Since for all these patterns $f = 1$ we need one more test pattern, say 000, to detect f/1 faults.

Karpovsky M.G., Yarmolik V.N. "TESTABILITY MEASURES AND TEST COMPLEXITIES FOR TESTING WITH INTERNAL ACCESS", Proc. IEEE WORKSHOP ON IDDQ TESTING, 1995 pp 9-14

TEST COMPLEXITES FOR IDDQ

- FOR UNATE 2-LEVEL NETWORKS

  $m+1 \leq T \leq m+2$

- FOR AND, OR TREES

  $T \leq 1.5 \lceil \log_2 m \rceil + 2$

- FOR XOR TREES

  $T \leq 2 \lceil \log_2 m \rceil + 1$

- FOR LINEAR XOR NETWORKS

  $T \leq m$

- FOR ADDERS OR MULTIPLIES (m-bits) AND I/O BFs

  $T = \lceil \log_2 m \rceil + 3$

FAULT COVERAGES

Let w_i is a number of ones in ith row of H

Then ith test pattern detects

N single stuck-at faults (SSFs)

and $w_i(N-w_i)$ bridging faults (BFs)

Average number of faults detected by one test pattern:

$$\left(w_i = \frac{N}{2}\right) \qquad N + \frac{N^2}{2} - \frac{N^2}{4} = N + \frac{N^2}{4}$$

The fraction of BFs detected by i randomly selected test patterns

$$1 - 2^{-i}$$

$T = 8$ or 9 is sufficient

TESTABILITY MEASURES

Local measure for detection of a BF between z_i and z_j

$$C(z_i, z_j) = \text{Prob}\{z_i \oplus z_j = 1\}$$

If $C(z_i, z_j)$ close to 1, then this BF has a good testability

$$|E(z_i) - E(z_j)| \leq C(z_i, z_j) \leq 1 - |E(z_i) - E(\bar{z}_j)|$$

$E(z_i) = \text{Prob}\{z_i = 1\}$ - signal probability

$C(z_i, z_j)$ is difficult to compute

$$C_{AVE}(z_i, z_j) = E(z_i)E(\bar{z}_j) + E(\bar{z}_i)E(z_j)$$

- If $E(z_i) = 1/2$, then

  $C_{AVE}(z_i, z_j) = 1/2$ for any z_j

- If $E(z_i) = 1$, then

  $C_{AVE}(1, z_j) = 1 - E(z_j)$

- If $E(z_i) = 0$

  $C_{AVE}(0, z_j) = E(z_j)$

Expected number T of test patterns:

$$\sum_{i>j} (1 - c(z_i, z_j))^T \geq \binom{N}{2}(1 - fc)$$

where fc is a fault coverage for BFs.

To simplify computations we replace $c(z_i, z_j)$ by $c_{AVE}(z_i, z_j)$

Global Testability measure

$$C = \binom{N}{2}^{-1} \sum_{i>j} C_{AVE}(z_i, z_j)$$

$$= \binom{N}{2}^{-1} \left(N_0 N_1 - \sum_i E(z_i)(1 - E(z_i)) \right)$$

where $N_0 = \sum_{i=1}^{N} E(z_i)$

$N_1 = N - N_0$

Computing of C is of the order $O(N)$ after computing signal probabilities

<u>Denote</u>

$$R = N_0 N_1 - \sum_{i=1}^{N} E(z_i)(1 - E(z_j))$$

R is a <u>global</u> testability measure

Then

$$\sum_{i>j} (1-c)^T \leq \binom{N}{2} (1-fc)_j$$

$$\binom{N}{2}\left(1 - \binom{N}{2}^{-1} R\right)^T \leq \binom{N}{2}(1-fc)$$

$$T \geq \left\lceil \left(\log_2 (1-fc)\right)\left(\log_2 \left(1 - \binom{N}{2}^{-1} R\right)\right)^{-1} \right\rceil$$

EXAMPLE: 8 AND

1. TREE IMPLEMENTATION

$R = 47.8$, $T = 7.7$,

$T_{min} = 6$

2. 1-dim IMPLEMENTATION

$R = 44.8$ $T = 8.4$

$T_{min} = 9$

Conclusion

FOR MOST DEVICES FEW IDDQ TESTS DRASTICALLY IMPROVE FAULT COVERAGES OF SSFs and BFs.

IDDQ TESTS DETECT SOME FAULTS undetectable by voltage testing.

IDDQ should be used together with voltage tests.