Testing of Special classes of Gates

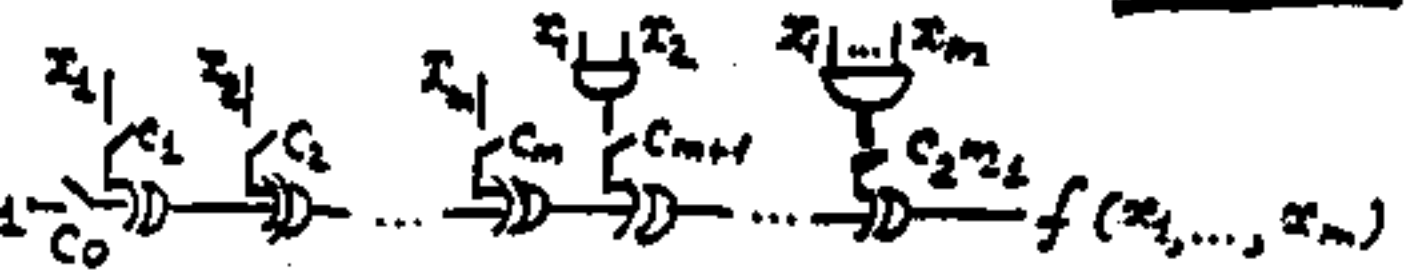
1. Reed-Muller Canonical Networks

T1. Any Boolean function $f(x_1,\dots,x_m)$ can be represented in the RM form:

$$f(x_1,\dots,x_m) = c_0 \oplus c_1 x_1 \oplus \dots \oplus c_m x_m \oplus c_{m+1} x_1 x_2 \oplus \dots \oplus c_{2^m-1} x_1 x_2 \dots x_m$$

(XOR's of products of arguments without negations; $c_i \in \{0,1\}$)

Reed-Muller Implementations: **UNIVERSAL**



$T(m)$ - minimal number of test patterns for detection of all single stuck-at faults in RM networks

Th2 $T(m) \le 3m+4$ ⟹ very good testability

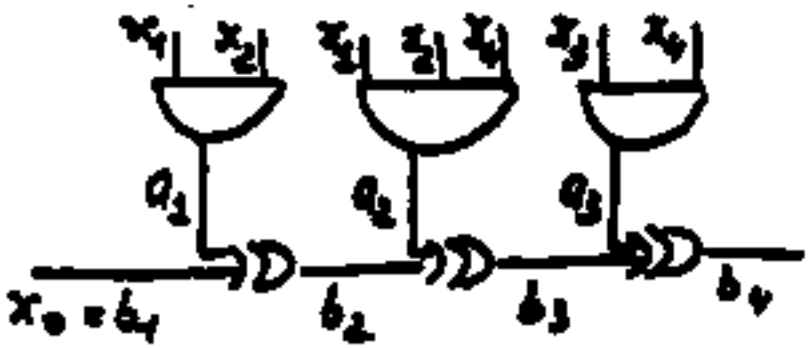
faults at fanout branches are detected
distinguish between branches

(K.K. Saluja, S.M. Reddy, IEEE TC, C-23, pp 552-554, 1974)

T3 If we don't distinguish between faults at fanout branches:

$T(m) = 2m+3$

Example



Test: x_0 x_1 x_2 x_3 x_4	Faults detected
0 0 0 0 0	$b_i/1$, $a_i/1$
1 1 1 1 1	$b_2/0$, $b_3/0$, $a_i/0$
0 1 1 1 1	$b_2/0$, $b_4/0$
0 1 1 0 0	$x_1/0$, $x_2/0$
0 1 0 0 0	$x_2/1$
0 0 1 0 0	$x_1/1$
0 0 0 1 1	$x_3/0$, $x_4/0$
0 0 0 1 0	$x_4/1$
0 0 0 0 1	$x_3/1$

RM NETWORKS ARE OPTIMAL FROM TESTING POINT OF VIEW.

2. Fanout-free networks NOT UNIVERSAL

** Th 1 $2\sqrt{m} \leq T(m) \leq m+1$

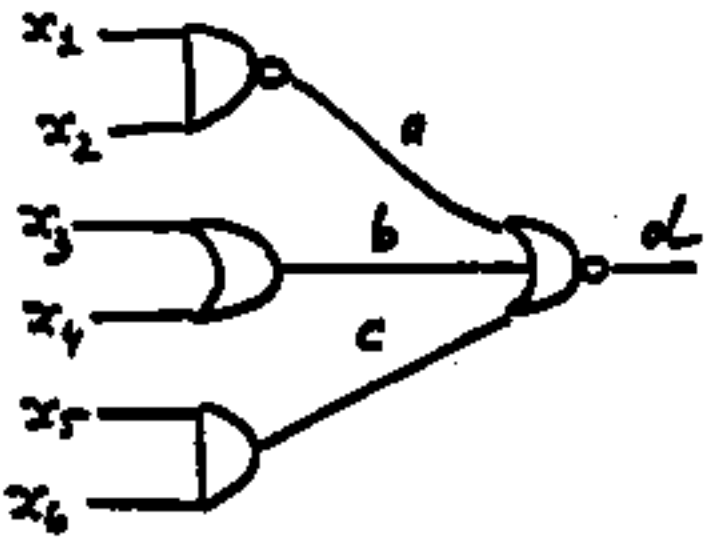
For SSFs and NAND gates

Th 2 For any FF network there exists a minimal single stuck-at fault test which also detects all multiple faults

(J. P. Hayes, IEEETC, C-20, pp 1496-1506 Dec 1981)

PATH SENSITIZATION

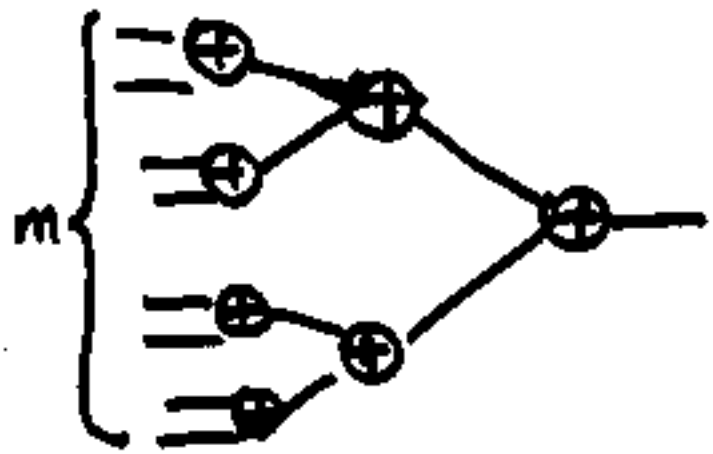
Example



Test: x_1	x_2	x_3	x_4	x_5	x_6	Faults detected:
1	1	0	0	0	0	$x_1/0$, $x_2/0$, $x_3/1$, $x_4/1$ a/1, b/1, d/0, c/1
0	1	0	0	0	0	$x_1/1$, a/0, d/1
1	0	0	0	0	0	$x_2/1$
1	1	0	0	1	1	$x_5/0$, c/0, $x_6/0$
1	1	0	0	0	1	$x_5/1$, $x_3/1$, $x_4/1$
1	1	0	0	1	0	$x_6/1$
1	1	1	0	0	0	b/0, $x_3/0$
1	1	0	1	0	0	$x_4/0$

IF A TEST DETECTS ALL INPUT STUCK-AT FAULTS, THEN THE SAME TEST DETECTS ALL INTERNAL STUCK-AT FAULTS

TESTING OF PARITY CHECKERS TREES



T1 FOR SSFs T(m)=3

J.P. HAYES "On Realization of Boolean Functions Requiring a Min Number of Tests" IEEE TRANS COMPUT. DEC. 1971

FOR PARITY TREES

T2. FOR DOUBLE STUCK-AT FAULTS SSF test has coverage $\simeq 83.33\%$.

S. Mourad, E.J. McCluskey, "Testability of Parity CHECKERS", IEEE Trans INDUSTRIAL ELECTRONICS, MAY, 1983

T3. FOR detection of all multiple stuck-at faults

$$T(m) = m + 1$$

TEST:

0 0 0 ... 0 0 0
0 0 0 ... 0 0 1
0 0 0 ... 0 1 0
. . . . . .
0 1 0 ... 0 0 0
1 0 0 ... 0 0 0

T1. THE SAME TEST DETECTS ALL AND OR BRIDGING FAULTS.

Internal Fanout-Free Networks — UNIVERSAL

Experimental Results

1. Any Single Fault Detection Test detects about 98% of all multiple faults with a multiplicity at most 6 (for 2-level AND-OR networks about 100%)

2. Inclusion of one fanout reduces up to 5% fault coverage for multiple faults

Conclusion: move fanouts to primary inputs

3. Almost all 2-level AND-OR Networks

$T(m) \simeq 2^{m-1}$, $T(m,N) \leq m+N+1$

N = # of product terms

4. $m \times 2^m$ decoders

$T(m) = 2^m$

5. $m \times 1$ Multiplexers

$T(m) \leq 2m$

6. K out of m networks

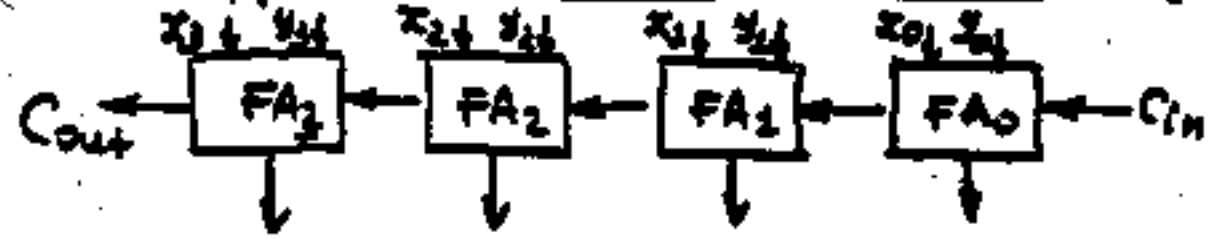
$T(m) \leq 2\lceil \frac{m}{K} \rceil$ $K = m/2$

output = 1 ⇔  ≥ K inputs equal 1

7. m-bit parity checkers in a form of 2-level AND-OR networks

$T(m) = 2^{m-1} + 1$

3. Ripple Carry Adders / Subtractors (BIT-SLICE DEVICES)



	x_3	y_3	x_2	y_2	x_1	y_1	x_0	y_0	C_{in}	Inputs to FA_i
t_1	0	0	0	0	0	0	0	0	0	000
t_2	1	1	0	0	1	1	0	0	1	001, ieven; 110, iodd
t_3	0	1	0	1	0	1	0	1	0	010
t_4	0	1	0	1	0	1	0	1	1	011
t_5	1	0	1	0	1	0	1	0	0	100
t_6	1	0	1	0	1	0	1	0	1	101
t_7	0	0	1	1	0	0	1	1	0	110, ieven; 001, iodd
t_8	1	1	1	1	1	1	1	1	1	111

$T(m) = 8$ for any m

$t_1 \div t_8$ detect all stuck-at faults in FA's, at the inputs of every FA all possible 8 vectors

Let $\mathbb{0} = (0, 0, \ldots, 0)$

$\mathbb{1} = (1, 1, \ldots, 1)$

$a = (1, 0, 1, 0, 1, 0, \ldots, 1, 0)$

$\bar{a} = (0, 1, 0, 1, 0, 1, \ldots, 0, 1)$

Then we have the following test for adders

	x	y	c_{in}
t1	$\mathbb{0}$	$\mathbb{0}$	0
t2	a	a	1
t3	$\mathbb{0}$	$\mathbb{1}$	0
t4	$\mathbb{0}$	$\mathbb{1}$	1
t5	$\mathbb{1}$	$\mathbb{0}$	0
t6	$\mathbb{1}$	$\mathbb{0}$	1
t7	$\bar{a}$	$\bar{a}$	0
t8	$\mathbb{1}$	$\mathbb{1}$	1.

9. UNIFORM NAND TREES

p - number of inputs per gate

d - number of levels in the tree

$$T(m) = p^{\lfloor d/2 \rfloor} + p^{\lfloor d+1/2 \rfloor} \simeq 2\sqrt{m}$$

(J.P. Hayes, IEEETC, C-20, pp 1496-1506 Dec. 1981)

TERMINAL I/O Faults of ANY MULTIPLICITY

$2(m-r) \leq T(m) \leq 2m-4$ $\quad m>3$?

$$r \geq \log_2(m-r), \quad r \propto \lfloor \log_2 m \rfloor$$

(S.M Reddy, T.C. Kuhl, IEEETC C-27, May 1978, pp 467-469)

TOTAL NUMBER OF MULTIPLE FAULTS IS: $3^m - 1$