Relationship between TESTING AND DESIGN VERIFICATION

DESIGN VERIFICATION is FOR man-made design errors

TESTING is FOR physical defects

- FOR physical defects (faults) one can develop fault models Then faults can be enumerated and the quality of a test can be estimate by the fault coverage

- FOR design errors the space of errors is not enumerable in most cases.
It is difficult to estimate a quality of a design verification procedure

Typical design errors are related to the sequencing of the data transfers and transformations rather than to the data operations, since DATA OPERATIONS ARE "LOCAL".

Most design verification procedures are based on SIMULATION

PROBLEMS:

1. Generation of input patterns
2. Estimation of results of verification (correctness of the design)
3. Estimation of completeness of test.
4. Simulation time.

A system which passes the design verification is shown to be correct only with respect to the test applied

Completeness of the test cannot be rigorously determined.

TEST GENERATION FOR DESIGN VERIFICATION is generally a heuristic process

FOR LSI/VLSI devices DESIGN VERIFICATION is very IMPORTANT (high cost of design error)

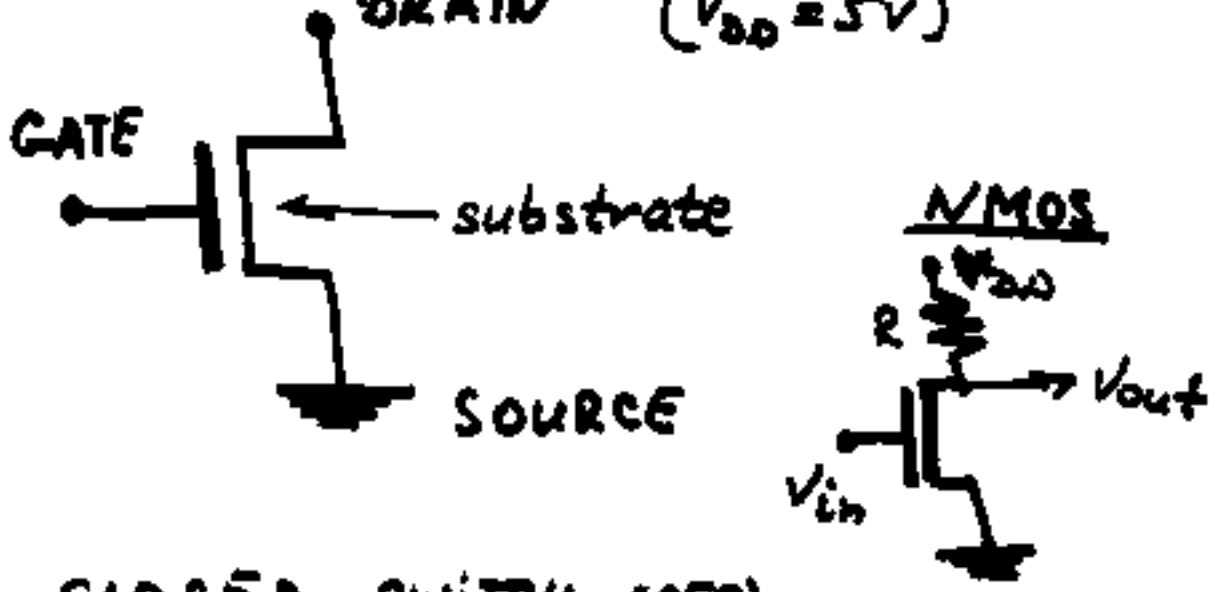
HIERARCHICAL DESIGN VERIFICATION:

1. HIGHEST-LEVEL FORMAL MODEL (e.g. RTL model) is checked against the INITIAL INFORMAL model
2. HIGHER-LEVEL MODEL defines a specification for its implementation at the lower level

3. Checking the lower level implementation is reduced to verification of this specification. This can be obtained by applying the same tests to the higher and lower level models; and the results from the higher-level model are expected results for the lower-level model.

(Saseki et al. "Hierarchical design verification for large digital systems", Proc. 18th Design Autation Conf. pp105-112, 1981)

TRANSISTORS



1. CLOSED SWITCH (OFF)

   VOLTAGE AT GATE 0

   NO CURRENT FROM V_{DD} through R.

   HIGH VOLTAGE AT OUTPUT

2. OPEN SWITCH (ON)

   INPUT VOLTAGE AT GATE V_{DD}

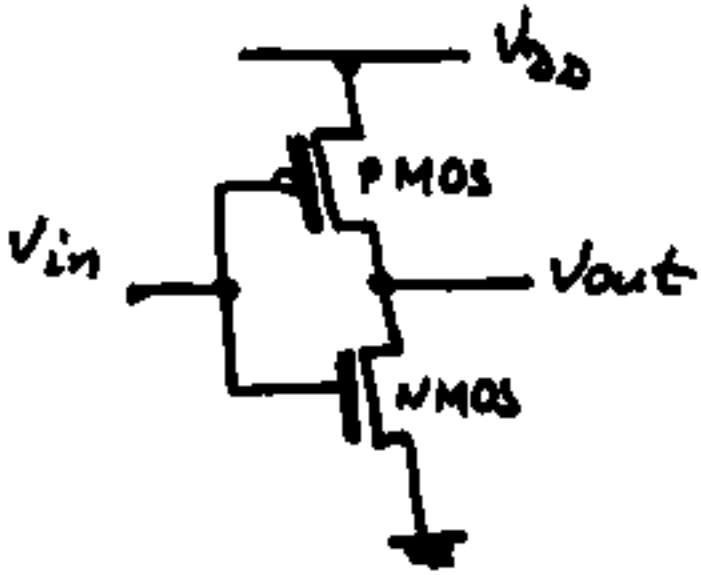
   current FROM V_{DD} through R.

   LOW VOLTAGE AT OUTPUT

N. Jha, S. Kundu "Testing and Reliable Design of CMOS Circuits" Kluwer Publishers, 1990

CMOS TRANSISTOR LOGIC (STATIC)

COMPLIMETARY LOGIC



INVERTER

If V_{in} high

NMOS CONDUCTS

PMOS NONCONDUCTIVE

V_{out} low

$V_{out} = \overline{V_{IN}}$

If V_{IN} LOW

NMOS NON CONDUCTIVE

PMOS CONDUCTIVE

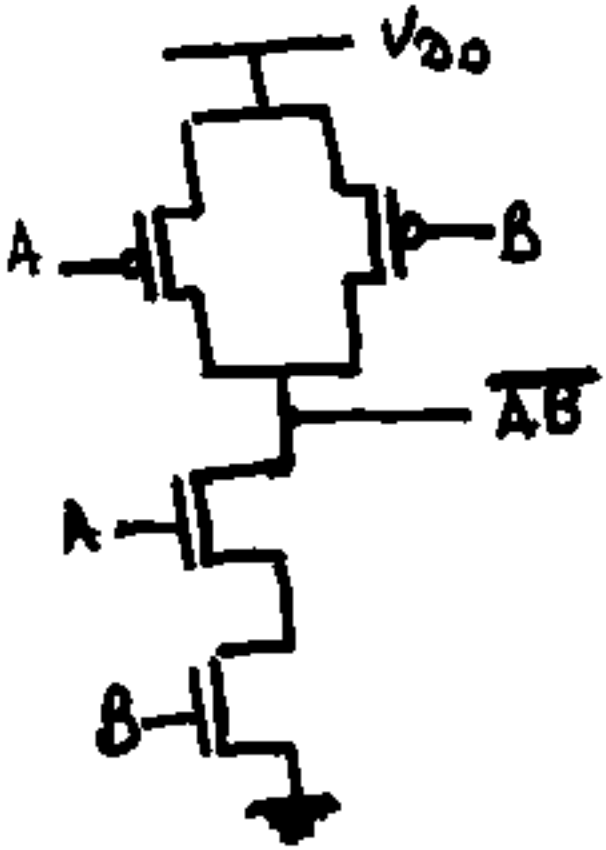
V_{out} high.

CMOS LOGIC

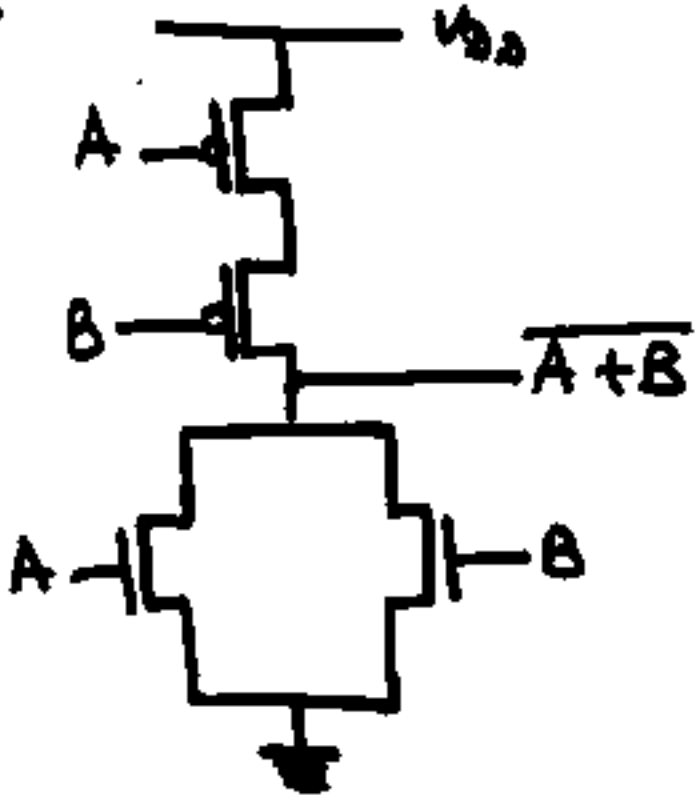
Advantages for high density chips:

- LOW POWER CONSUMPTION
- HIGH NOISE IMMUNITY
  (MAX NOISE VOLTAGE WHICH CAN BE TOLERATED)
- ONLY one transistor conducts at any time.
  Little current from V_{DD} to ground. Low heat dissipation
  Most faults results in THE DRASTIC INCREASE OF THIS current (IDDQ TEST)
- both transistors ARE PARTIALLY ON DURING THE SWITCHIN OPERATION

CMOS NAND (STATIC)

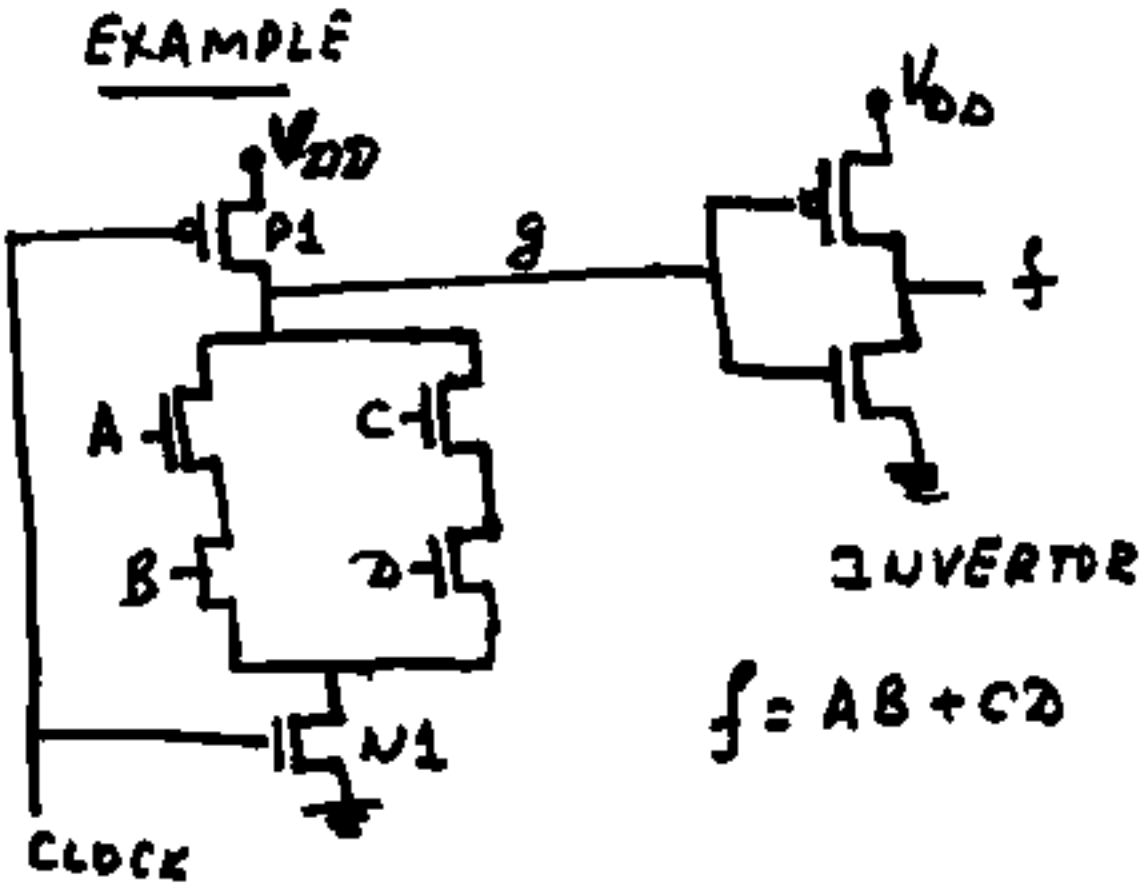


CMOS NOR



DYNAMIC CMOS (DOMINO)

EXAMPLE



$f = AB + CD$

If CLOCK=0 P1 conducts and precharge $g \Rightarrow f = 0$ (precharge phase)

If clock = 1 N1 conducts (evaluation phase) $\Rightarrow$

$f = AB + CD$

- EVERY COMPLEX GATE IS FOLLOWED by INVERTOR
- Outputs of inverters = 0 during precharge phase.
- primary INPUTS (A, B, C, D) are changed only during precharge phase.
- DOMINO CMOS requires less area on the chip than STATIC CMOS.
- DOMINO may require more power than static (for precharging
- DOMINO is FULLY COMPATIBLE WITH STATIC CMOS