TEST ECONOMICS

	COST OF DETECTION OF ONE FAULT
1. CHIP TEST (MANUFACTURING)	\$1,00
2. BOARD TEST	\$10,00
3. SYSTEM TEST (FIELD)	\$100,00
4. COMPUTER NETWORK TEST	\$1000,00

PROBLEMS:

FAULT-DETECTION

FAULT-DIAGNOSIS

- 1 -

TEST ECONOMICS

Relation between defect levels (DL) yields (Y) and fault coverages (C)

DL – fraction of devices shipped which are defective

EXPERIMENTAL RESULT

$$DL = 1 - Y^{1-C} \quad (1)$$

Examples

1) $C = 1 \Rightarrow DL = 0$

2) $Y = 1 \Rightarrow DL = 0$

3) $Y = 0.2,\ C = 0.987 \Rightarrow DL = 0.02$

T.W. Williams, N.C. Brown, "Defect Level as a Function of Fault Coverage", IEEE TC C-30, N12, 1981, pp 987-988.

From (1)

$$C = 1 - \frac{\lg(1-DL)}{\lg Y} \qquad (2)$$

<u>Example</u> $Y = 0.1$, $DL = 0.02 \Rightarrow$

$$C = 1 - \frac{\lg(1-0.02)}{\lg 0.1} = 1 - 0.0088 = 0.9912$$

Cost curve for testing.

Importance of a low defect level:

For a board with 70 components and

$DL = 0.01$ / component

Prob. of getting a fault-free board: $(1-0.01)^{70} = 0.4$.

Q - number of components

RELIABILITY → $R = (1 - DL)^Q$

$$\sqrt[Q]{R} = 1 - DL$$

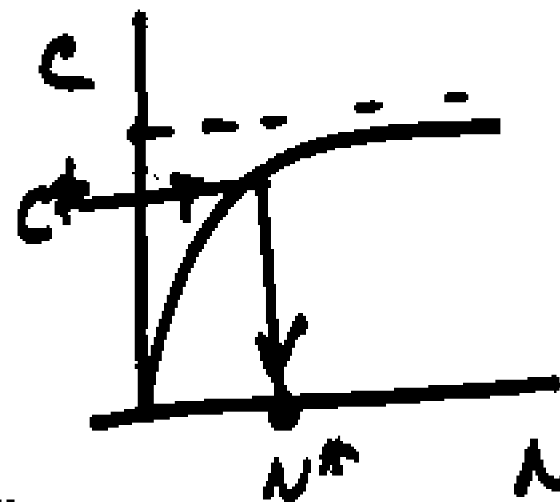
$$DL = 1 - \sqrt[Q]{R}.$$

Y - yield

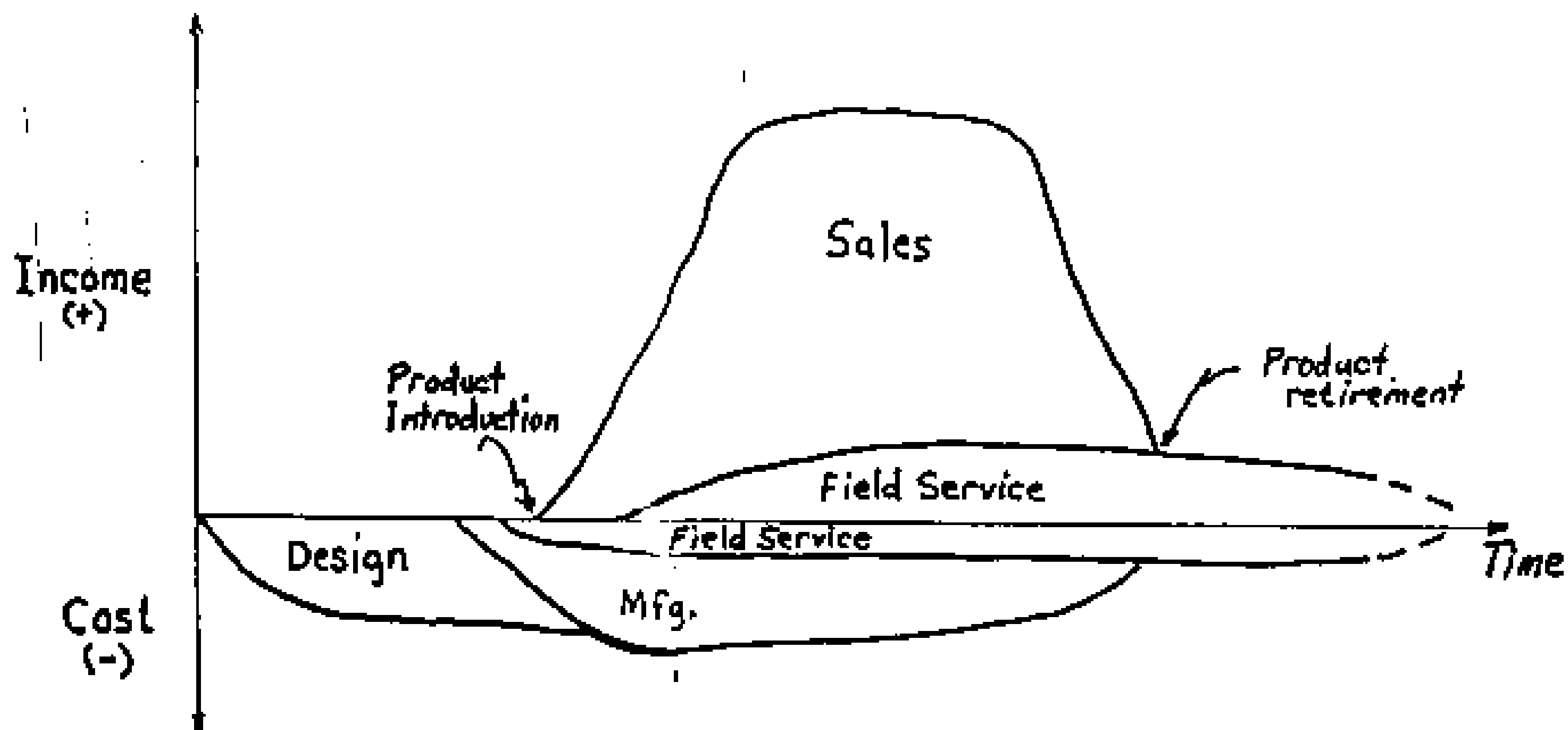
$$C^* = 1 - \frac{\log(1 - DL)}{\log Y} = 1 - \frac{\log(1 - 1 + \sqrt[Q]{R})}{\log Y}$$

fault coverage / component

$$C^* = 1 - \frac{\log \sqrt[Q]{R}}{\log Y} =$$



$$\boxed{C^* = 1 - \frac{\frac{1}{Q}\log R}{\log Y}.}$$



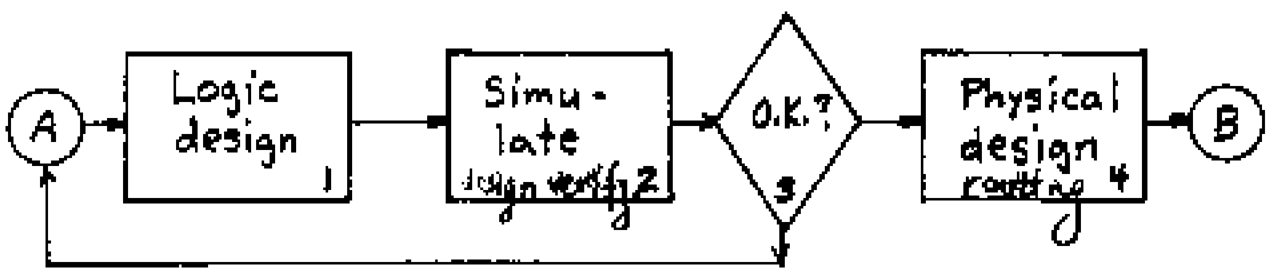
Observations:

o [illegible] time of product introduction, and costs.

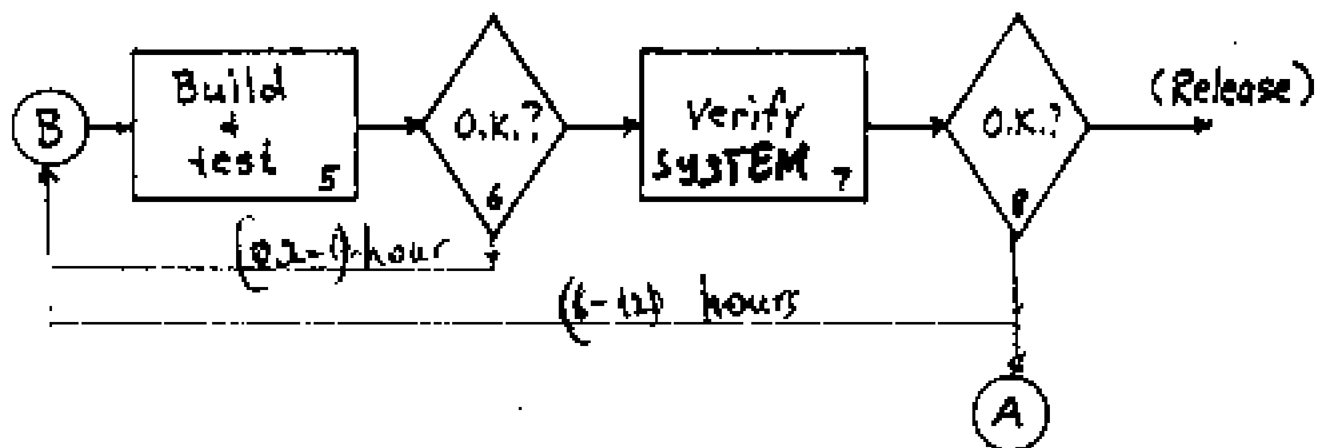
o New technology and the competition controls time of product retirement.

Product Life-Cycle Cost and Revenue

Hardware Design Process and Impact of Test on Time-to Market



(Engineering Prototype)



NOTES:
Path from 8 to 1 for design errors
Path from 8 to 5 for construction errors
Loop time 8-5-8 is 6 to 12 hours
Loop time 6-5-6 is .3 to 1 hours

If early test process quality is low, traveling the path 8-5-8 many times means that time to market can be impacted 3 to 6 months.

Environment of change

From development thru the first year of shipment, constant change is the norm!

Product and test change impact:
- Interruption of Mfg. cycle
- Temporary quality degradation
- Cost, morale impact
- Lower "ramp-up" rate

Example: VAX 8600 development vs. change time

initial test development
- chip: 500-gate array
  - test gen. - days
- module: 20-25 K gates, RAMs
  - test gen. - months
- system: 20 modules
  - test gen. - years

test changes, turnaround time
- chip: days - no problem
- module: 1 to 4 weeks
- system: 1 to 4 months

Note: in the latter two, hardware can change faster than the tests can.

VAX-8600* 1400 design errors
50 man years for μdiagnostic of CPU.

Conclusion

Testing is a key element [redacted] to deliver competitive, high quality products to the marketplace at the right time.

FOR IBM ES/9000

about 60 hours of simulation

Test sequences of 152 megabytes

Stages in the Development and Testing of a System

Stage	Error sources	Error Detection TOOLS
Specification, LOGIC design	Algorithm design, specifications	Simulation Consistency checks
Prototype construction	Wiring, assembly, timing, components	Stimulus/response test
Manufacture	wiring, assembly, components	System test, Diagnostics
Installation	Assembly, Components	System test, Diagnostics
Operational	Components AGING, environmental fluctuations	Off-line field test, functional test, random test, BUILT-IN-TEST.

TYPES OF TESTING

CRITERIA	ATTRIBUTE OF METHOD	TERMINOLOGY
when testing performed?	• concurrently with computing • nonconcurrent	• On-line Off-line
Where is a source of stimuli?	• within a device • external tester	• BIST • External testing
what is tested?	• IC • BOARD • SYSTEM • NETWORK	
How are stimuli and responses produced?	• Retrieved from storage • Generated during testing	• Stored pattern testing • Algorithmic testing, comparison testing

TYPES OF TESTING (CONT'D)

CRITERIA	ATTRIBUTE OF METHOD	TERMINOLOGY
How are stimuli applied?	• FIXED ORDER • DEPENDING ON THE RESULTS OBT.	 Adaptive
How fast are stimuli applied?	• SLOWER THAN NORMAL SPEED • AT NORMAL SPEED	• Static test • at-speed test
What are the observed results?	• output patterns • COMPRESSED RESPONSES	 • COMPACT TEST SIGNATURE ANALYSIS
What lines are accessible for testing?	• ONLY I/O • I/O and INTERNAL LINES	• Edge-pin test • GUIDED PROBE BED-OF-NAILS ELECTRON BEAM IN-CIRCUIT TEST CROSSCHECKS
Who checks the results?	• THE DEVICE-UNDER TEST ITSELF • external tester	• SELF-TEST • SELF-CHECKING BIST • EXTERNAL TEST