3.1

Gate-level Testing

Complexity of test generation

Test generation time for any program generating a minimal test is growing exponentially with an increase in a number of gates even for detection of single stuck-at faults

Test Generation is a NP-HARD problem-no polynomial time algorithm.

(O.H. Ibarra, S.K. Sahni, IEEETC, C-24, pp242-249 1975)

Experimental Results for SSF

$$t \simeq c N^3$$

t is a time for test generation

N is a number of gates in DUT

C is a constant

(T. W. Williams, K. P. Parker, IEEETC, C-31, N1 pp 2-15, 1982)

ERROR MODELS

I. CHIP-LEVEL MODELS

Let $\hat{Z}$ is test response matrix

$\hat{Z}$ is $(T \times n)$ binary matrix

Similarly Z is $(T \times n)$ binary matrix of fault free responses

and $E = \hat{Z} \oplus Z$ is an error matrix

T is a number of test patterns

n is a number of primary outputs.

Then $E = [e(1)\ e(2) \ldots]$

$$E = \begin{bmatrix} e(1) \\ e(2) \\ \vdots \\ e(T) \end{bmatrix}$$

ERROR MODELS

1. Uniform errors

All $E \neq 0$ are equiprobable

2. Correlated errors

2.1. TEMPORAL MODELS

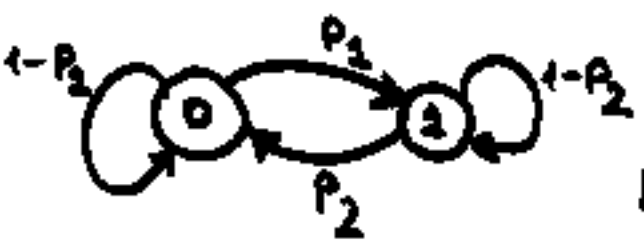
2.1.1. TIME INDEPENDENT ERRORS

$e(t)$ $(t = 1, 2, \ldots, T)$ are statistically independent

MOST POPULAR MODEL FOR COMBINATIONAL DEVICES, RANDOM TEST

2.1.2. TIME CORRELLATED ERRORS

MARKOV CHAIN MODEL.



0 - NO ERRORS
1 - ERROR.

$P_1 = \text{Prob}\{e(t+1) \neq 0 \mid e(t) = 0\}$

$P_2 = \text{Prob}\{e(t+1) = 0 \mid e(t) \neq 0\}$

difficult to COMPUTE (P_1, P_2)

2.2 SPATIAL MODELS

2.2.1. SPACE INDEPENDENT ERRORS

Let $\| e(t) \| = \ell$

$\| e(t) \|$ is number of ones in $e(t)$ (HAMMING NORM OF $e(t)$), number of bits at the output distorted at moment t.

FOR ANY t:

$$\text{Prob} \{ \| e(t) \| = \ell \} = \binom{n}{\ell} P_b^{\ell} (1-P_b)^{n-\ell}$$

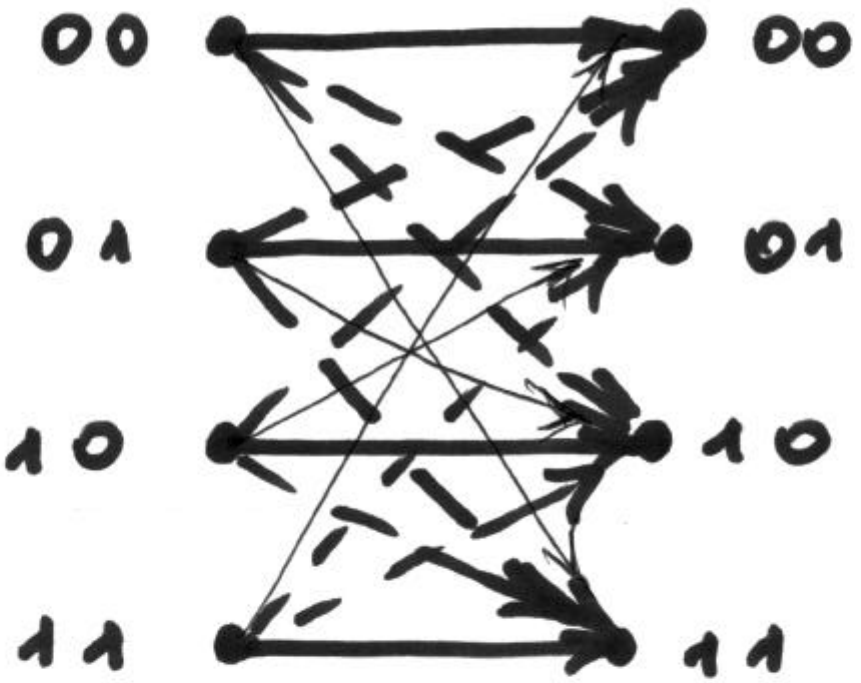
where P_b - bit distortion rate

Prob of $0 \to 1$ = Prob of $1 \to 0$ distortions

This model is efficient for networks with limited fanouts

INDEPENDENT ERRORS

n=2



FAULT FREE

FAULTY

$P_b(1-P_b)$

P_b^2

$1-2P_b(1-P_b)-P_b^2$

2.1.3. Burst errors (disks)

2.2.2. SPACE SYMMETRICAL MODEL

FOR ANY t:

All $e(t) \neq 0$ are equiprobable

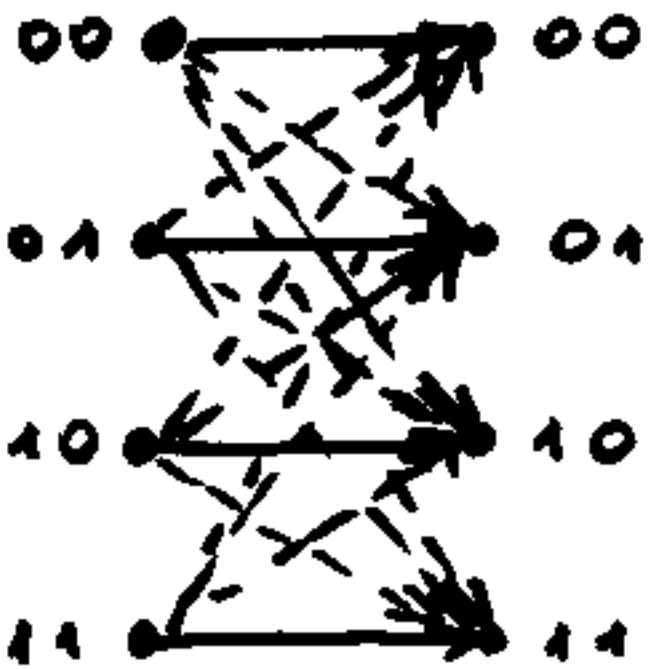
$$\text{Prob}\{e(t)=i\} = \begin{cases} 1-p & , i = 00\ldots0 \\ \frac{p}{2^n-1} & , i \neq 00\ldots0 \end{cases}$$

SPACE SYMMETRICAL MODEL
is very popular

This model is efficient for networks with large fanouts

Symmetrical ERRORS

n = 2



FAULT FREE

FAULTY

$1 - p$

$p/3$

2.2.3 SPACE ERRORS OF A GIVEN MAGNITUDE

FOR ANY t :

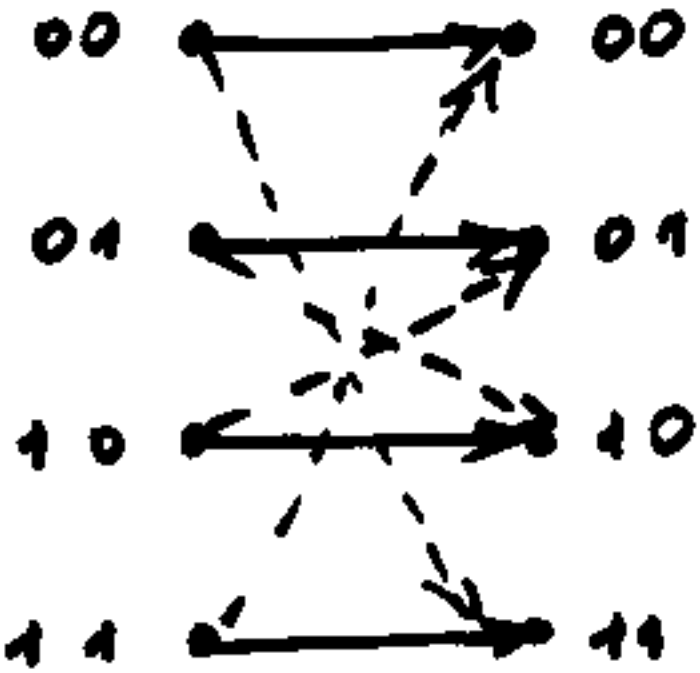
$$\text{Prob}\{e(t) = i\} = \begin{cases} 1-p, & i = \overbrace{a \ldots 0}^{n} \\ p, & i = a \\ 0, & \text{otherwise.} \end{cases}$$

for some n-bit vector a

This model is efficient for networks where every fault affects only a fixed set of outputs for all test patterns

ERRORS WITH FIXED MAGNITUDES

$n = 2$, $Q = (1,1)$



FAULT FREE

FAULTY

$1-p$

p

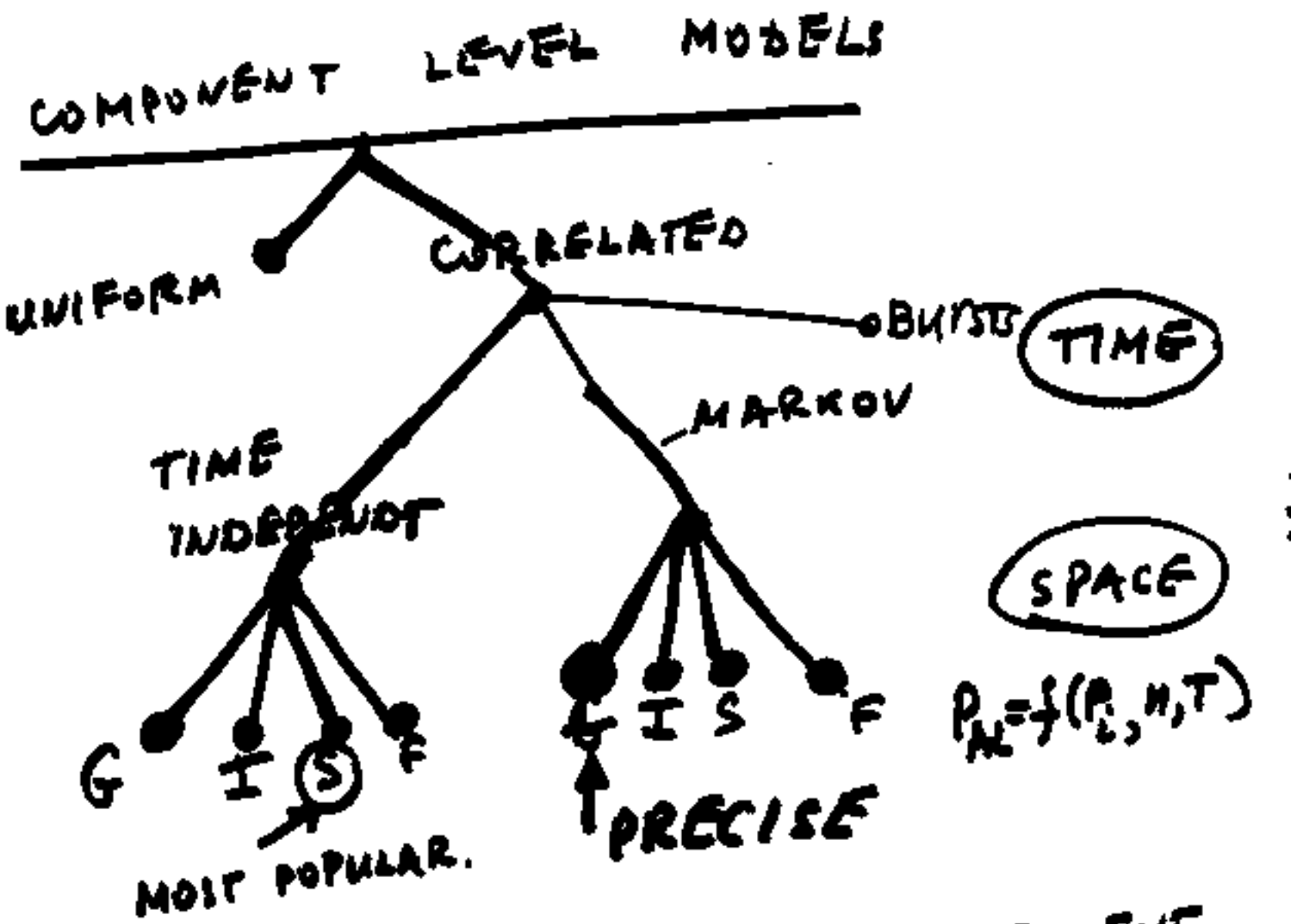
2.2.4. General spatial MODEL

$\{P_0, P_1, \ldots, P_{2^n-1}\}$ - error distribution in space

$P_0 = \text{Prob}\{e(t)=0\}$ no errors

$P_i = \text{Prob}\{e(t)=i\}$

Space error distribution is difficult to compute. It depends on a DUT and a test for the DUT.

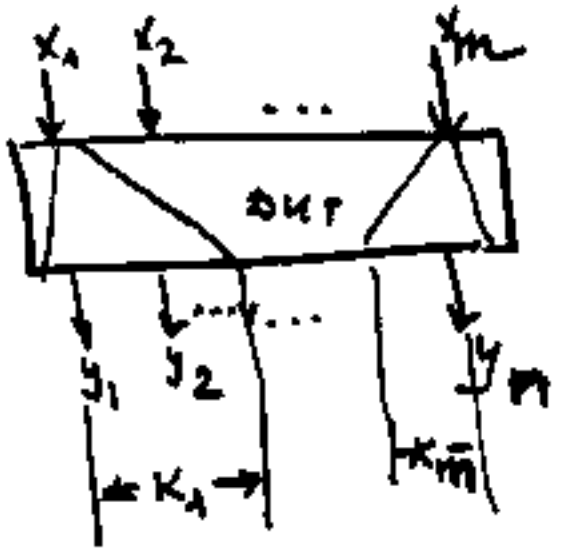


G- GENERAL, I-INDEPENDENT

S- SYMMETRICAL, F-FIXED MAGN.

COMPUTATION OF SPACE ERROR DISTRIBUTIONS

Let K_i outputs depend on x_i for the DUT



K_i is the size of dependence cone for input x_i ($i=1,2,\ldots,m$)

Then, the number of different error patterns N_e due to single stuck-at faults is upperbounded by

$$N_e \leq \sum_{i=1}^{m} (2^{K_i} - 1)$$

EXAMPLE: $m=32$, $n=32$, $\max K_i = 10$

$$N_e \leq 32 \cdot (2^{10} - 1) \qquad (<= 2^{32})$$

IMPROVEMENT FOR THE UPPER BOUND ON N_e

Let Y_i is the set of outputs that depend on input x_i $(i=1,2,\dots,m)$

Let $|Y_i| = K_i$, $|Y_i \cap Y_j| = K_{ij}$,

$|Y_i \cap Y_j \cap Y_r| = K_{ijr}$, ...

Then

$$N_e \le \sum_i (2^{K_i} - 1) - \sum_{i,j} (2^{K_{ij}} - 1) + \sum_{i,j,r} (2^{K_{ijr}} - 1) - \dots$$

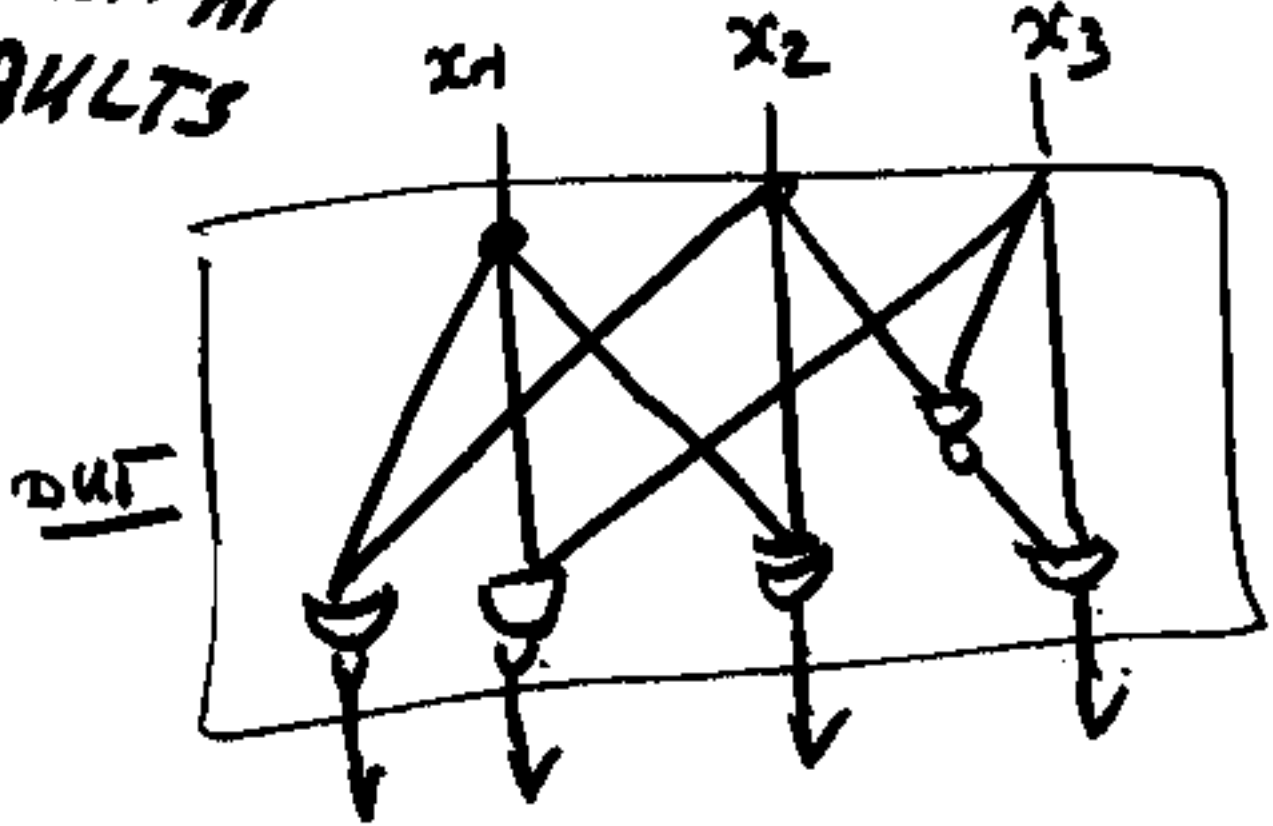
TIME INDEPENDENT, SPACE SYMMETRICAL MODEL ARE THE MOST POPULAR MODELS.

Example.

SINGLE STUCK-AT FAULTS

$P_{15} = 0$

$N_e \leq 18$



$k_1 = 3$

$k_2 = 3$

$k_3 = 2$

$N_e \leq (2^3 - 1) + (2^3 - 1) + (2^2 - 1)$

$k_{12} = 2$, $k_{13} = 1$, $k_{23} = 1$, $k_{123} = 1$.

$$N_e \leq \sum_i (2^{K_i} - 1) - \sum_{i,j} (2^{K_{ij}} - 1) +$$

$$+ \sum_{i,j,r} (2^{K_{ijr}} - 1) -$$

FOR THE PREVIOUS EXAMPLE

$$N_e \leq [(2^3-1) + (2^3-1) + (2^2-1)] - [(2^2-1) + (2^2-1) + (2^1-1)] + (2^0-1) = 13$$

Conclusions on chip level error models

1. For all time independent models for large test length T all the space error models converge to the same aliasing probability 2^{-r} (where r is a number of bit in the signature

2. FOR small T space independent model predicts maximum aliasing (pessimistic estimation) and space symmetrical model predicts minimum aliasing (optimistic estimation). Symmetric model predicts aliasing in large networks more precisely than other models

M.G. Karpovsky, S.K. Gupta, S.K. Pradhan

"UNIFORM [illegible] ANALYSIS OF ALIASING."

Proc. INT. TEST CONF. 1991.

BOARD OR SYSTEM LEVEL ERROR MODELS

1. Independent errors:

Prob of ℓ COMPONENT beeing faulty is $\binom{S}{\ell} p^{\ell} (1-p)^{S-\ell}$

where S - is the size of a board or system

p - prob of an error at the output of a component

(p can be computed by using one of chip level error models)

2. System CORRELATED ERRORS

Equiprobable single node failures

EXAMPLE : TREE PROCESSOR

Possible error patterns are:

1 0 0 0 0 0 0 0
0 1 0 0 0 0 0 0
0 0 1 0 0 0 0 0
0 0 0 1 0 0 0 0
0 0 0 0 1 0 0 0
0 0 0 0 0 1 0 0
0 0 0 0 0 0 1 0
0 0 0 0 0 0 0 1
1 1 0 0 0 0 0 0
0 0 1 1 0 0 0 0
0 0 0 0 1 1 0 0
1 1 1 1 0 0 0 0
0 0 0 0 1 1 1 1
1 1 1 1 1 1 1 1

in this table 1 indicates that output of the corresponding processor is distorted.

All errors due to a fault in a single node of in a single link are equiprobable.

ERRORS IN y_i are distributed ACCORDING TO ONE OF THE CHIP ERROR MODELS