DESIGN FOR TESTABILITY (DFT)

- AD HOC TECHNIQUES
- STRUCTURED TECHNIQUES
- METRICS ARE :
  - CONTROLLABILITY
  - OBSERVABILITY
  - [illegible]
  - TESTABILITY

T.W. Williams, K.P. Parker, "Design for Testability – A Survey," IEEE – TC, vol C-31, No. 1, Jan 1982

Guidelines

Structured (bit-sliced) design

Avoid random logic

- minimize redundant hardware

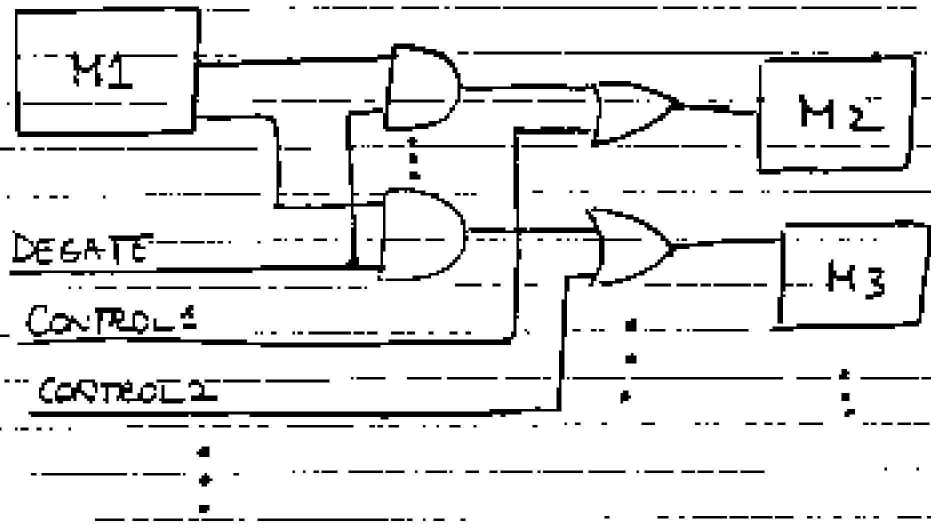
Avoid deep logic

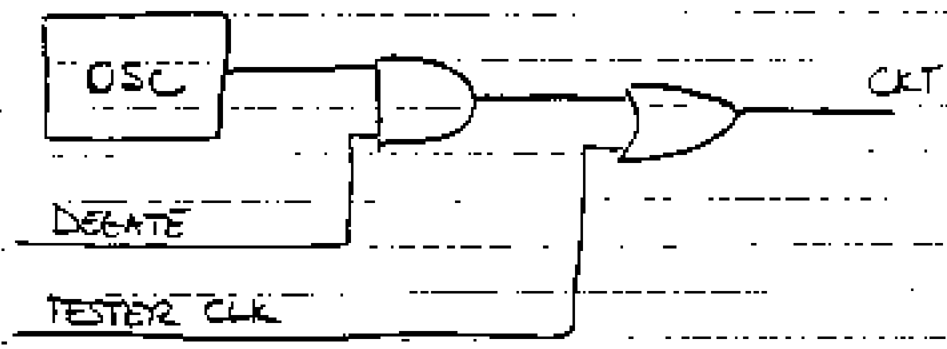
- use XOR gates (instead of OR)

- Avoid reconverging paths — THE MAJOR PROBLEM
- Avoid networks with many levels
- Avoid fanouts
  minimize a number of fanouts
- **Avoid asynchronous logic**
- Use LSSD or SCAN designs
  (reduce testing of sequential logic to **combinational one**)

DFT AD HOC TECHNIQUES (OFF-LINE)

• PARTITIONING & DEGATING

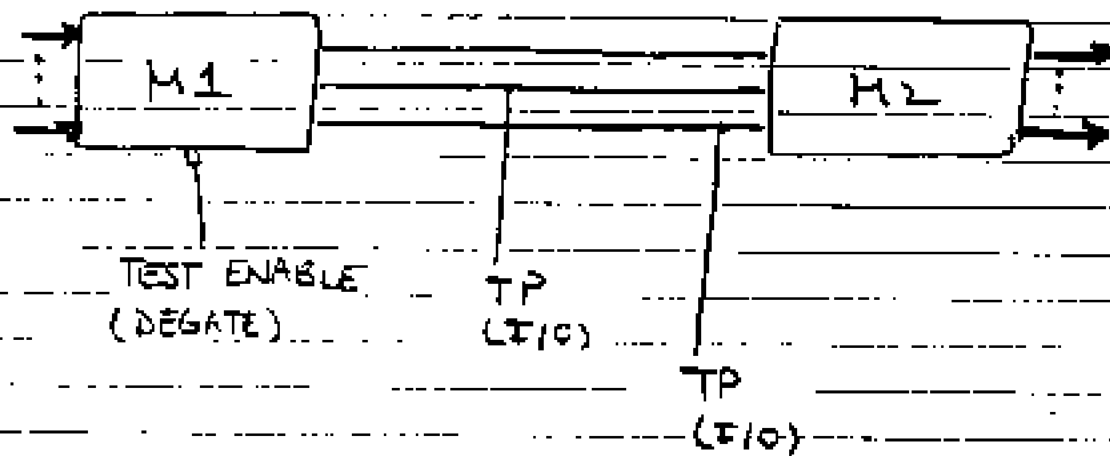




• IMPROVES CONTROLLABILITY

Akers, S.B., "Partitioning for testability", Jrnl Design Automation Fault Tolerant Computing, vol. 1, Feb. 1977

• TEST POINT INSERTION

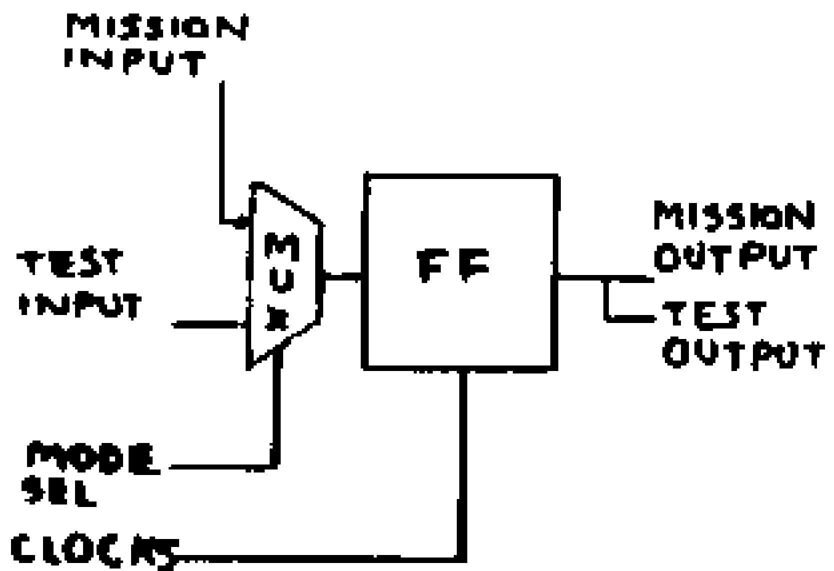


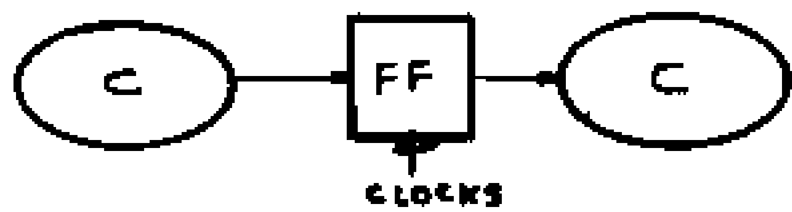
- IMPROVES OBSERVABILITY **FOR M1**
- IMPROVES CONTROLLABILITY **FOR M2**

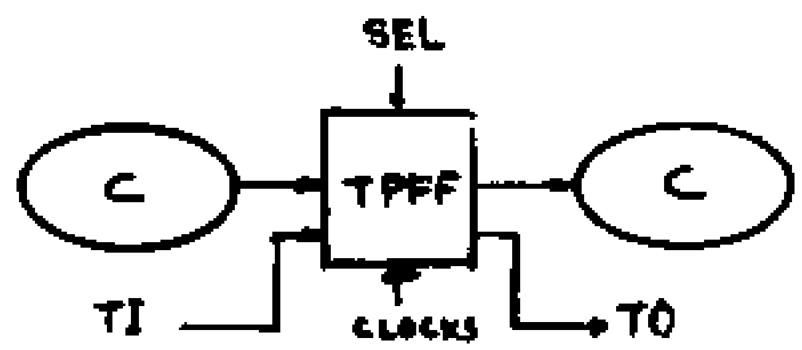
J.P. HAYES, "On Modifying logic networks to improve their diagnosability," IEEE-TC, vol. C-23, pp. 56-62, Jan. 1974.

M.J.Y. WILLIAMS, J.B. ANGELL, "Enhancing testability of LSI circuits via test points and additional logic," IEEE-TC vol. C-22, pp. 46-60, Jan. 1973

TEST POINT FLIP-FLOPS (TPFs)







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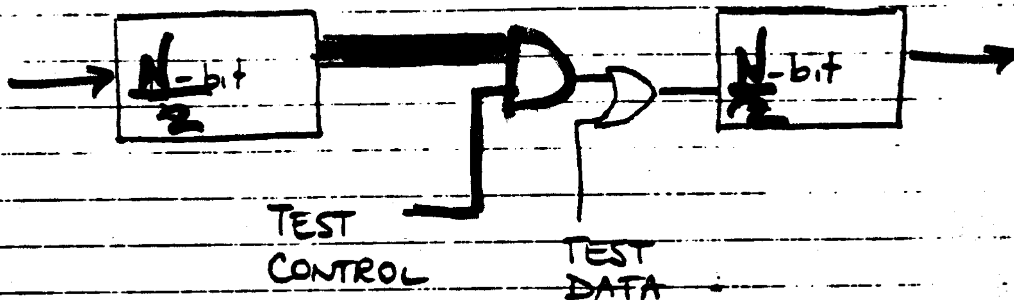
4. BREAK LONG COUNTER CHAINS



N-BIT COUNTER REQUIRES MAXIMUM OF 2^N CLOCKS

$\frac{N}{2}$-BIT " " " $2^{N/2}$

FOR A 16 BIT COUNTER $2^N = 64K$

$2^{N/2} = 256$

AVOID ASYNCHRONOUS LOGIC — **RACES AND HAZARDS**

- DIFFICULT TO DIAGNOSE
- FAULTS MAY INDUCE RACES — **DELAY FAULTS**
- DIFFICULT TO SYNCHRONIZE TESTER
- DIFFICULT TO FAULT SIMULATE

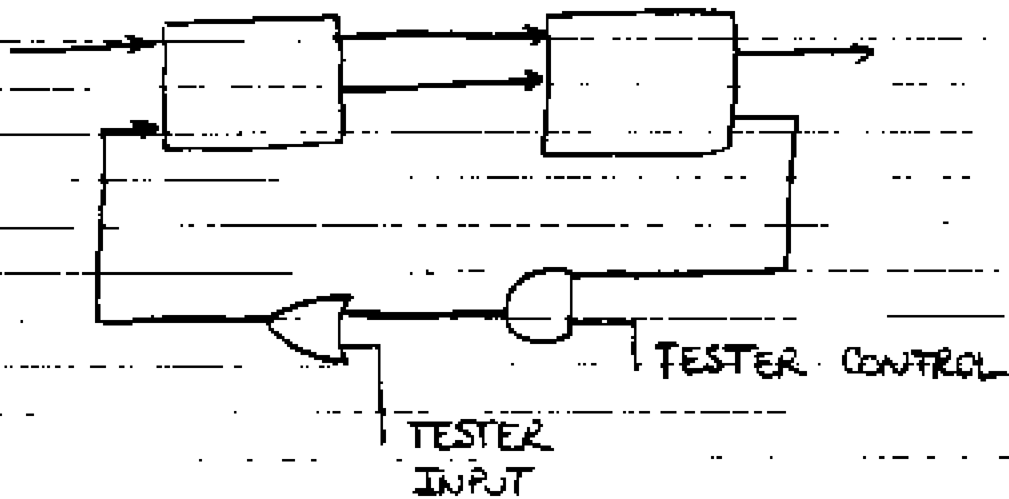
AVOID HIGH FANOUTS & RECONVERGENT PATHS

- DIFFICULT FOR ATG ALGORITHM

AVOID RANDOM LOGIC

- PLA
- ARRAY STRUCTURES
- BIT SLICED DESIGNS

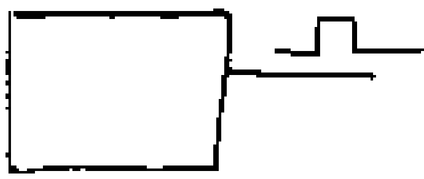
BREAK GLOBAL FEEDBACK LOOPS



3. <u>AVOID MONOSTABLE AND "ONE-SHOT" ELEMENTS</u> *or delay lines*

(THE "BANE" OF EVERY TEST ENGINEER!)

- DIFFICULT TO SYNCHRONIZE TO TESTER
- MAY BE DIFFICULT TO RESET/TRIGGER



MONOSTABLE OR ONE SHOT

I. AVOID USING "FINE TUNED" OR "CUSTOMIZED" COMPONENTS

- "TWEAKING" (HUMAN INTERACTION) REQUIRED "ON-LINE" (EXTRA TEST EQUIPMENT)
- OFTEN REQUIRES ADDITIONAL PARAMETRIC TESTING

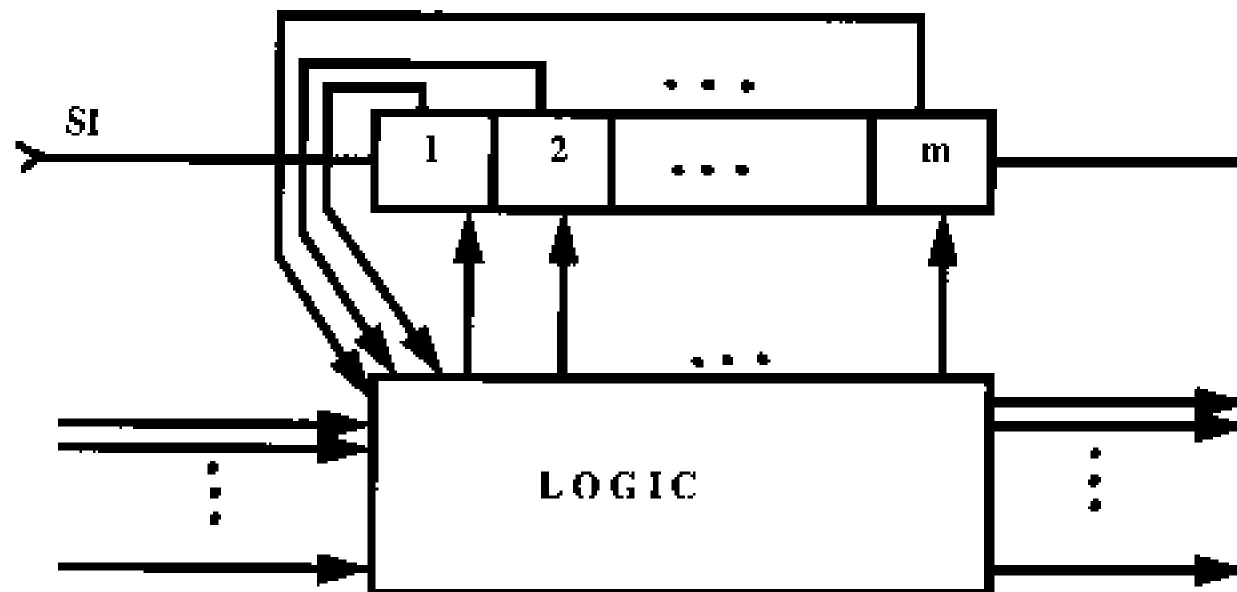
STRUCTURED DFT TECHNIQUES

- SCAN DESIGN
  - LSSD
  - SCAN PATH
  - RANDOM ACCESS SCAN
  - SCAN SET
  - GENERIC SCAN
- SIGNATURE ANALYSIS

GOAL:

- REDUCE ATG TO CL CASE
- OVERHEAD
- OFF-LINE vs ON-LINE SCAN TESTS

SCAN DESIGN

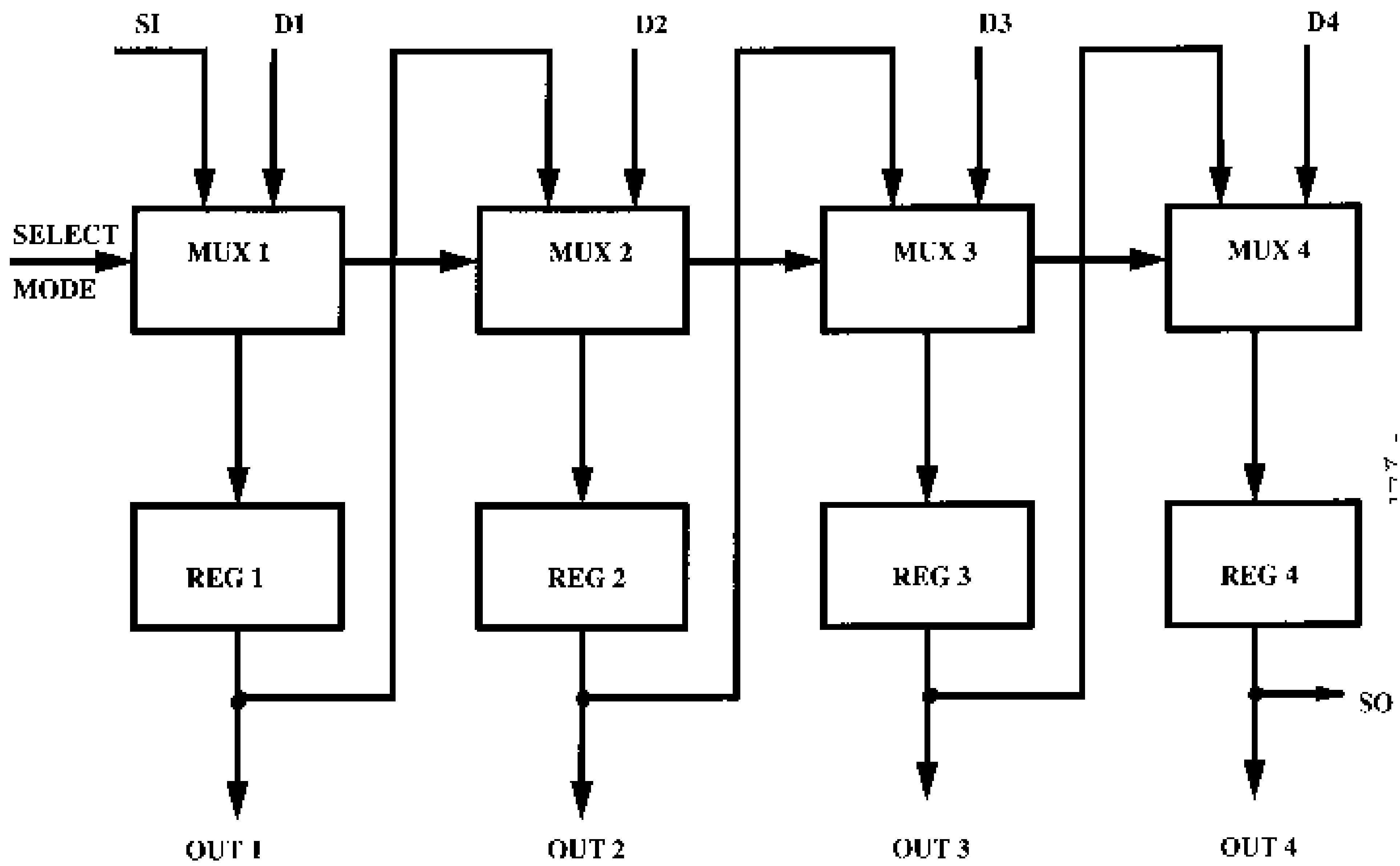


Features :

- Shift register not in data path (may be off chip !);
- " Snapshots " available of system operation;
- Negligible effect on system operation.

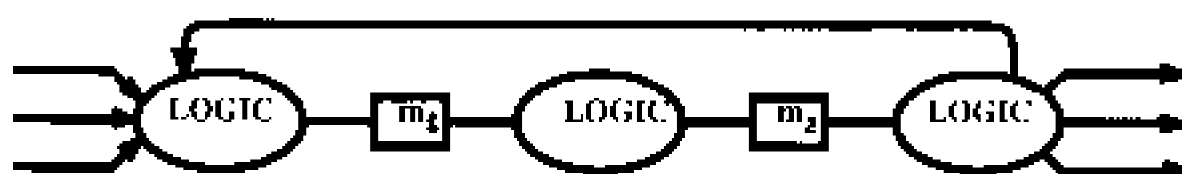
J.H.Stewart, " Future testing of large LSI circuit cards, ". Dig 1977, Semiconductor Test Sym., Oct. 1977, pp. 6 - 17.

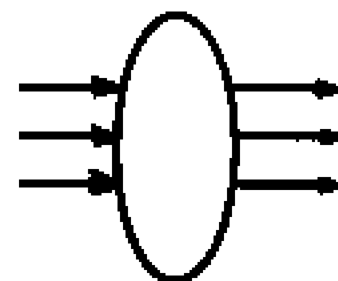
SCAN BY MULTI[illegible]XING



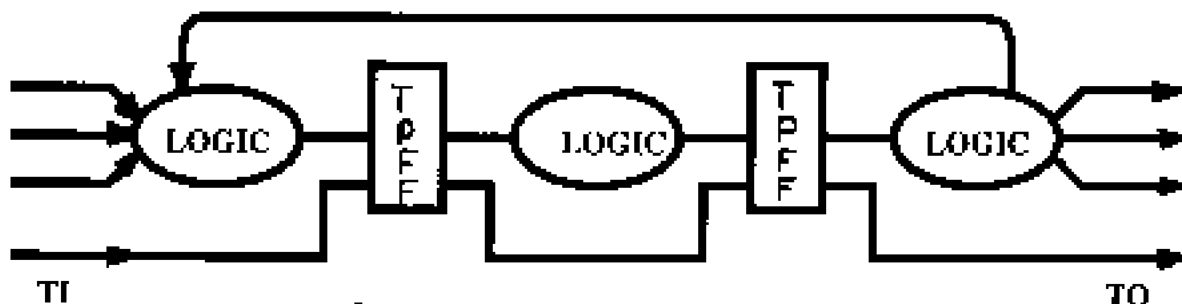
COMPLETE SCAN DESIGN

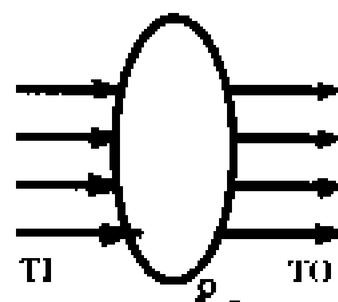
ORIGINAL



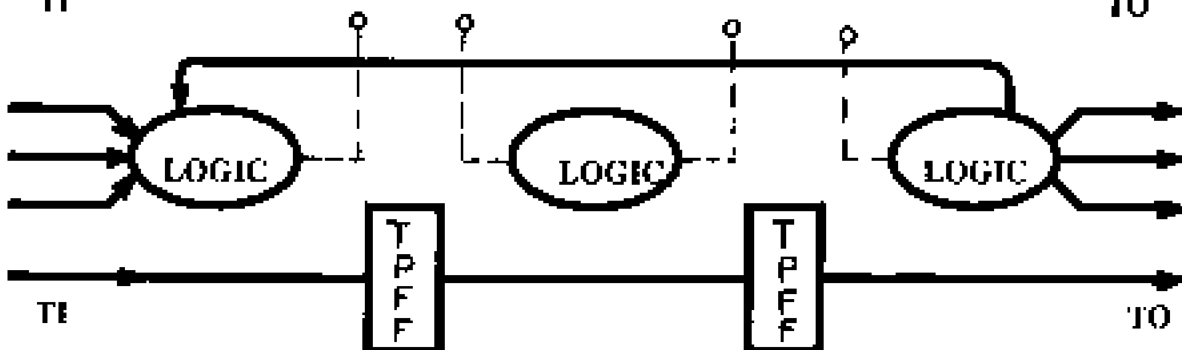


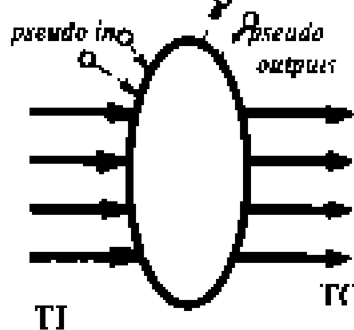
WITH
COMPLETE SCAN





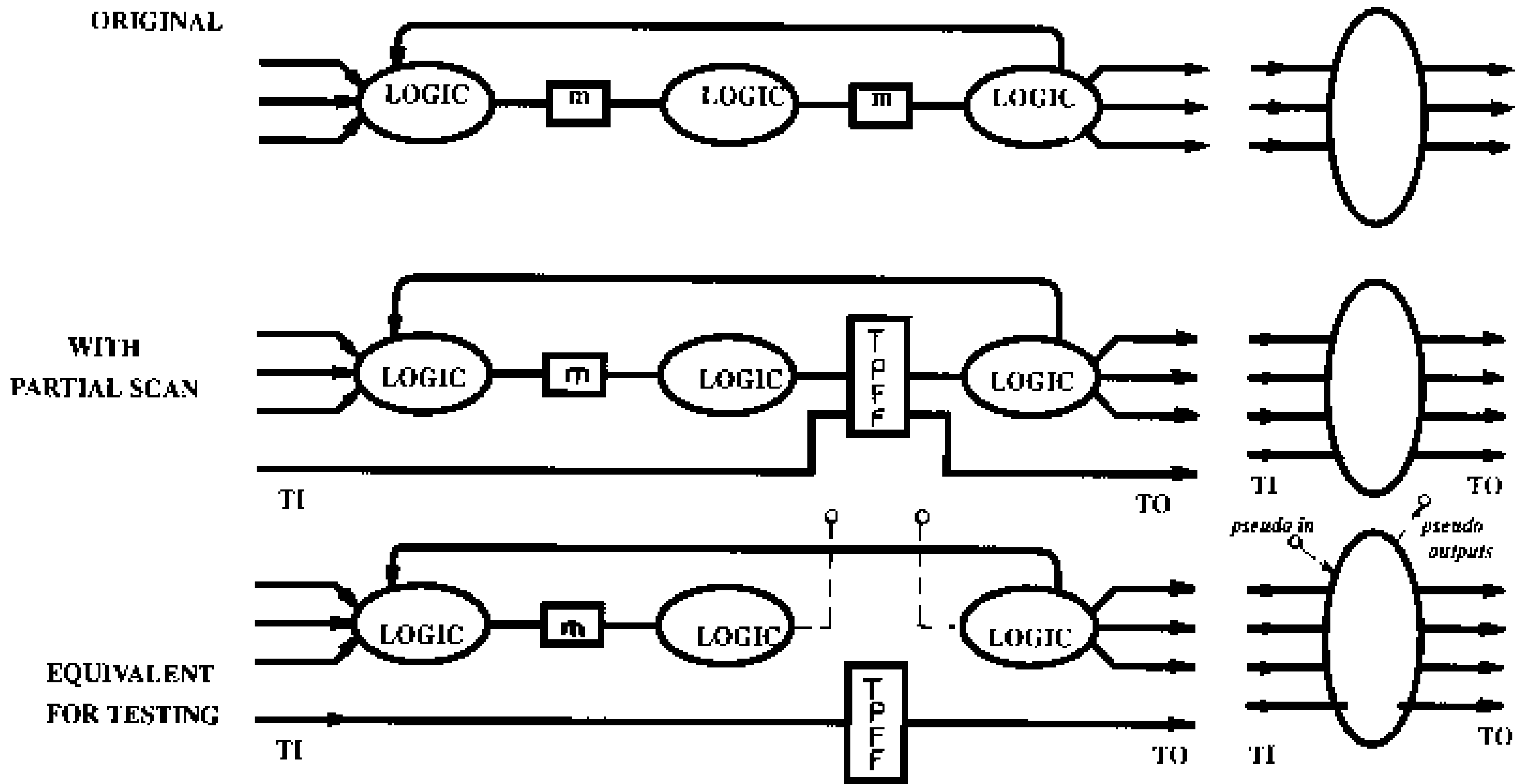
EQUIVALENT
FOR TESTING





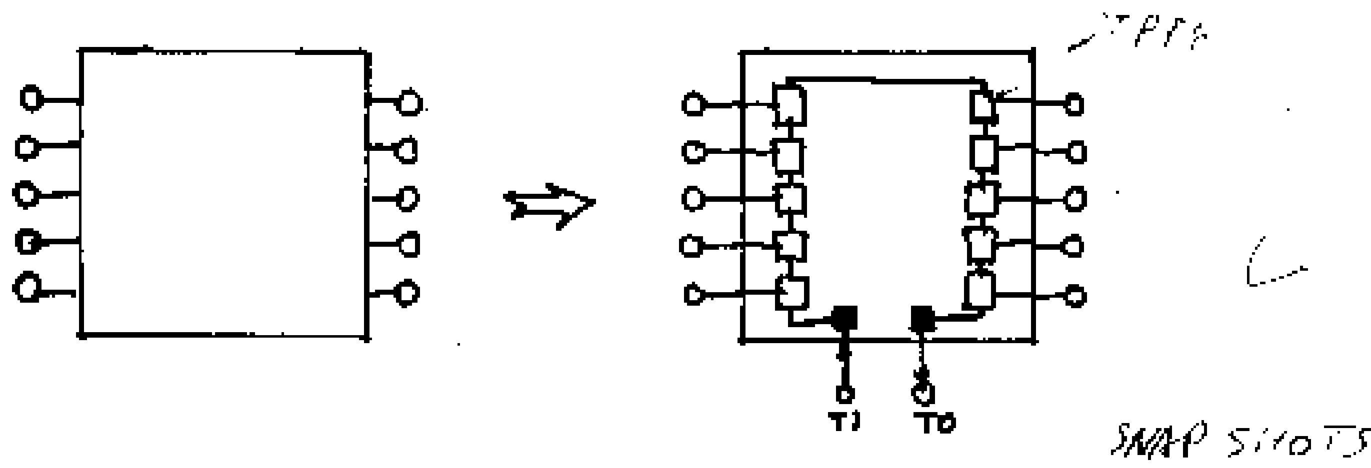
* Cost proportional to # of internal memory elements.

IN - COMPLETE SCAN DESIGN



* Cost proportional to # of internal loops.

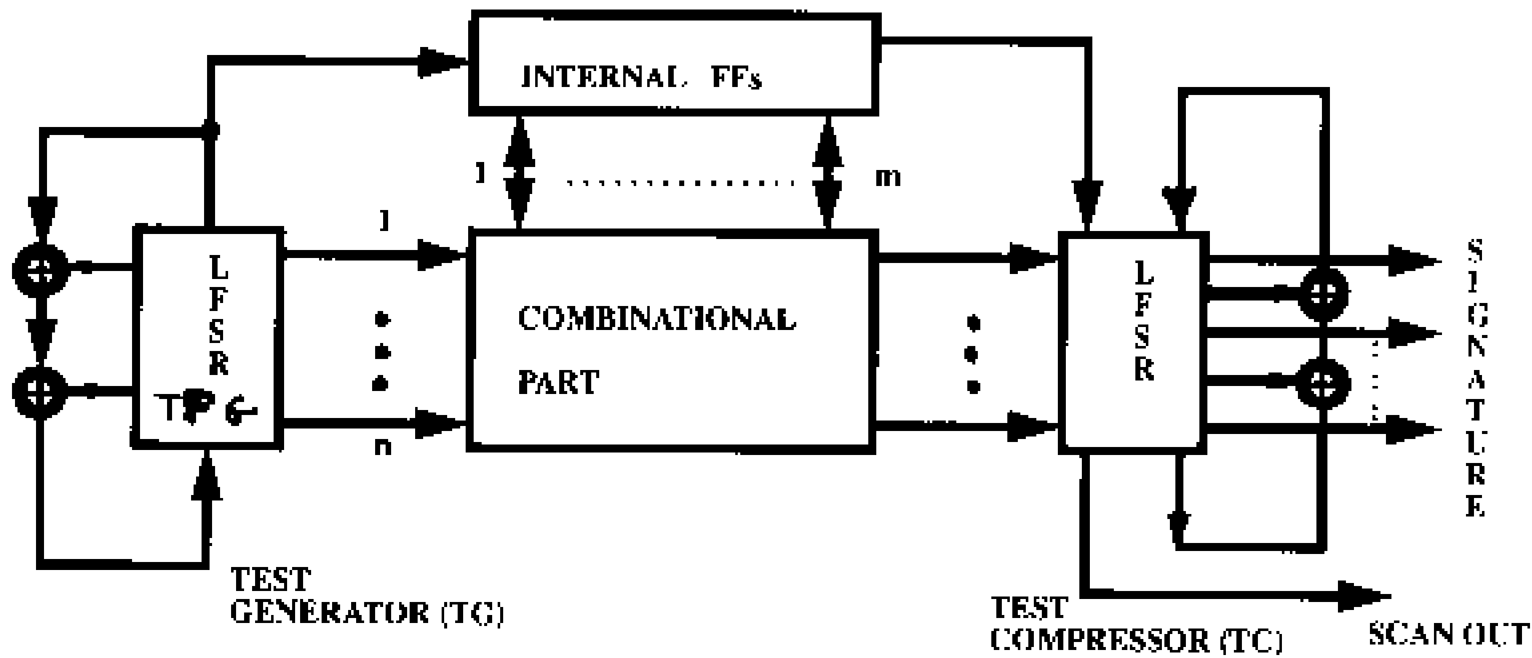
BOUNDARY SCAN (JTAG)



- **Cost Proportional to number of I/O pins/pads**
  - **Test Development portable to next assembly level**
  - **Aid to Wafer Probe and In-Situ Testing at all assembly level**
  - **Separability from Analogs etc..**
  - **Works around pin limited tester..**

BOUNDARY (I/0) SCAN WITH LFSRs.

FOR BIST

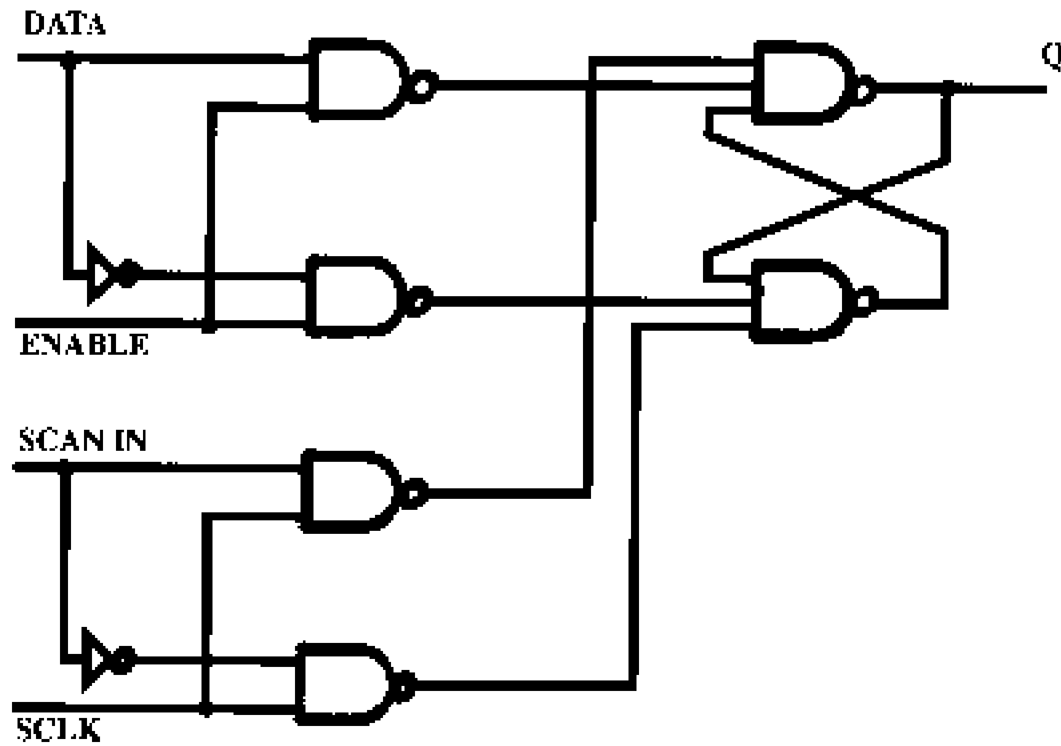


<u>Problem</u> : Maximize pattern coverage number of distinct (n + m) bit inputs to combinational part divided by $2^s - 1$ where s - number of bits in TG ($n \le s$)

Gloster, Brglez " Boundary SCAN with cellular based bist " Proc ITC, 1988, pp 138 - 145.

LEVEL SENSITIVE SCAN DESIGN (LSSD).

Level Sensitive SCAN Design (IBM).



Shift Register Latch (SRL), 2 clocks.

(*normal operation*)

DATA

ENABLE

SCAN IN

φ_a

φ_b

+ L1

+ L2

Overhead of L2 Latch.

D

ENABLE

SCAN IN

φ_a

L1

master

+ L1

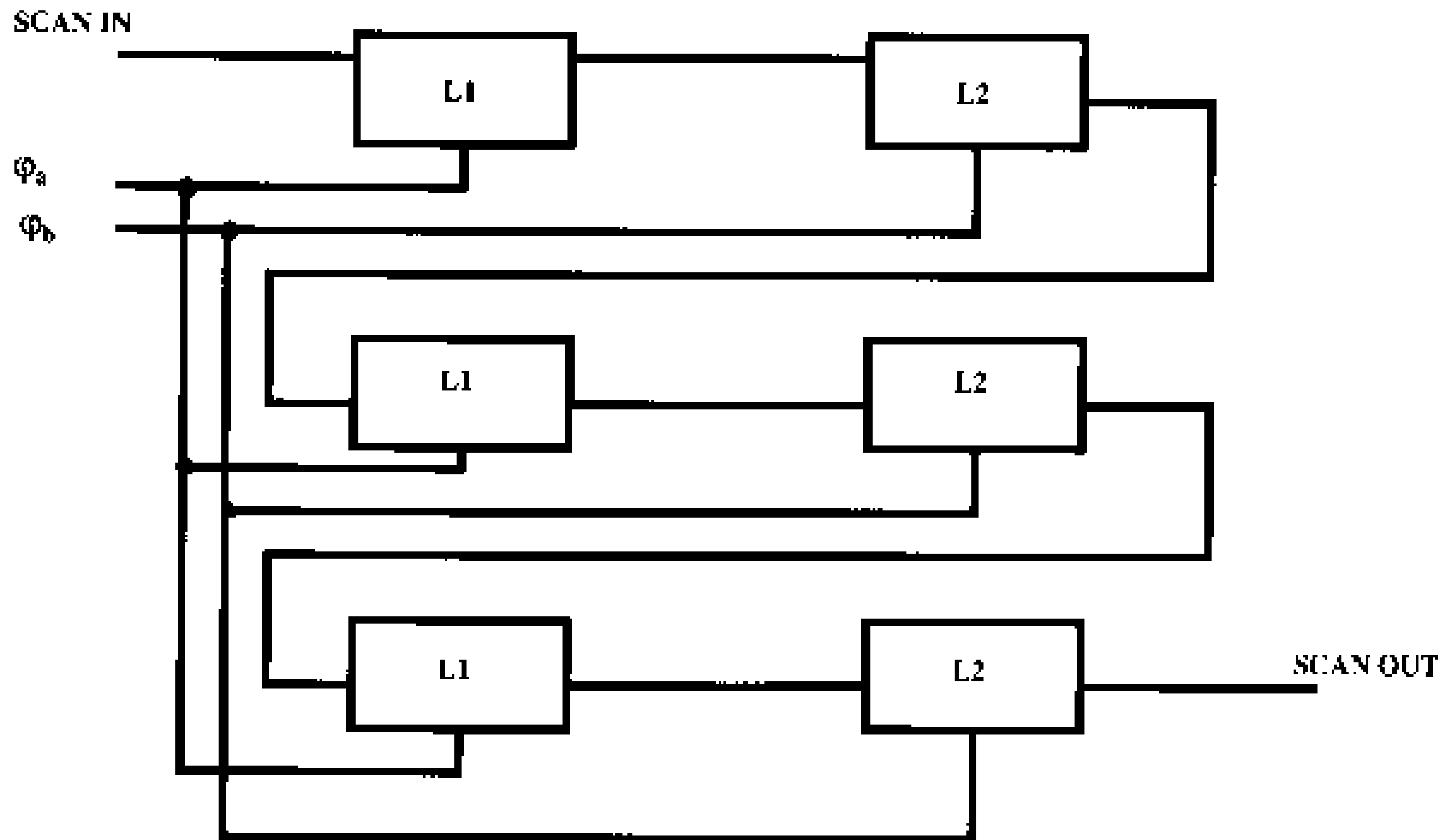
φ_b

L2

+ L2

slave

LEVEL SENSITIVE SCAN DESIGN (LSSD).



Modifications of SCAN.

Total(complete)SCAN --> 15% overhead;

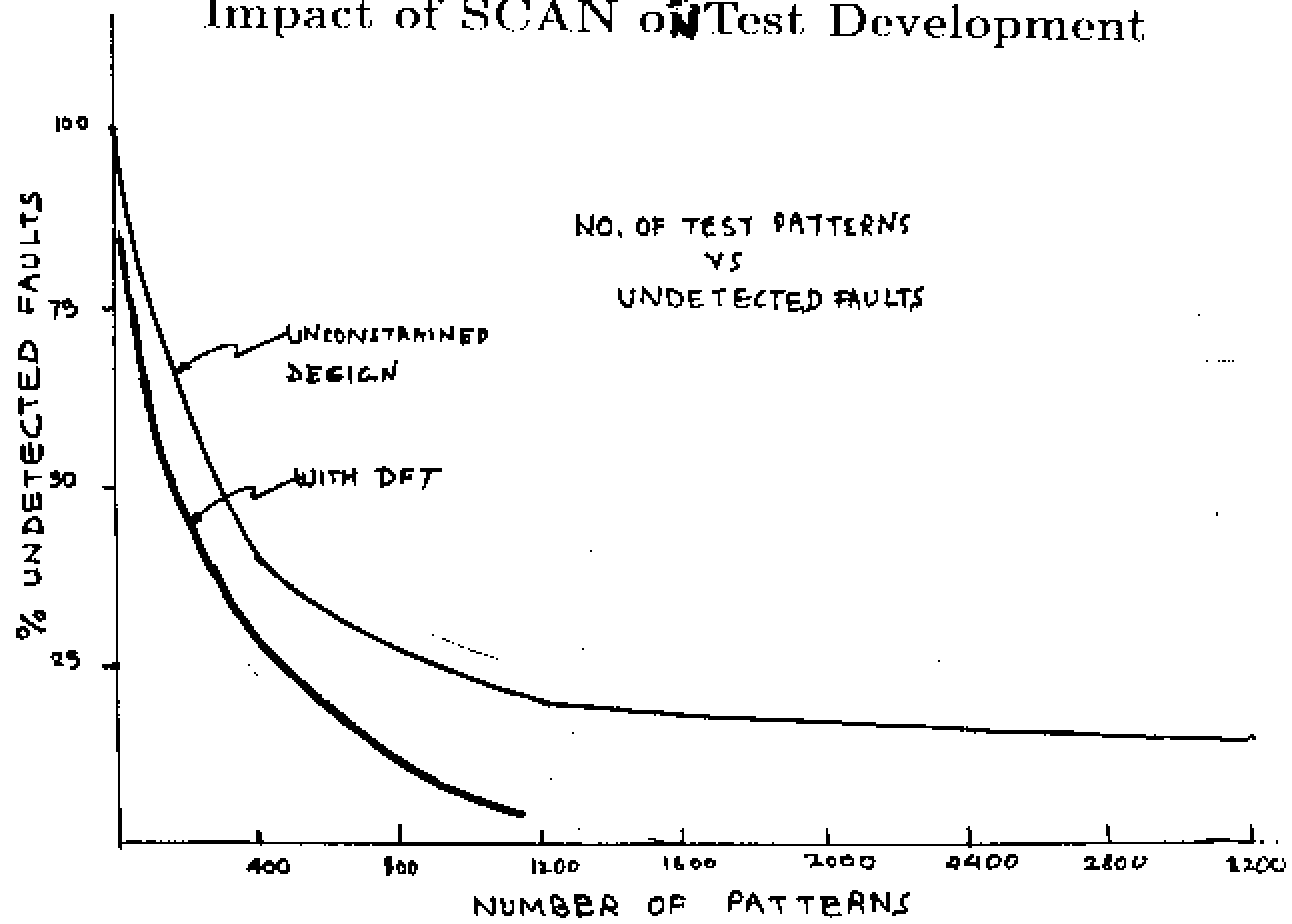
Partial(incomplete)SCAN;

I/O SCAN (boundary SCAN), JTAG;

RAM SCAN --> 80% overhead.

Solution of the pattern coverage problem can be found in :

P. Nagvajara, M. G. Karpovsky, L. B. Levitin
" Pseudorandom Test Patterns Generation for Boundary SCAN Design ",
Journal of Electronic Testing, March, 1991.


Impact of SCAN on Test Development
NO. OF TEST PATTERNS
VS
UNDETECTED FAULTS
UNCONSTRAINED
DESIGN
WITH DFT
% UNDETECTED FAULTS
100
75
50
25
400
800
1200
1600
2000
2400
2800
3200
NUMBER OF PATTERNS

SUMMARY. on DFT.

SCAN design offers many advantages in test development and testing during a products life cycle

- TPFs and SCAN paths for internal *Controllability*, *Observability*, etc.
- Complete SCAN offers maximum benefits but In-complete Scan can also offer significant testing advantages at reasonable costs

BiST offers quick, at-speed testing with minimal test data storage and handling

- POLYDIV (LFSR based) self-test most popular, effective, and economical
- Cost reduced by sharing with system hardware and by externally supporting the self-test control

SUMMARY...

- **POLYDIV BIST and Serial SCAN are** *Made For Each Other*
- **Techniques applicable at any level of design but costs favor that DFT Implementation begin at the chip level**
- **Testability Support Chips can facilitate DFT implementation at module/system level**
  - *Concatenable Polydivider* **chips, central self-test control chips, etc can help to reduce IC count and testability design effort**