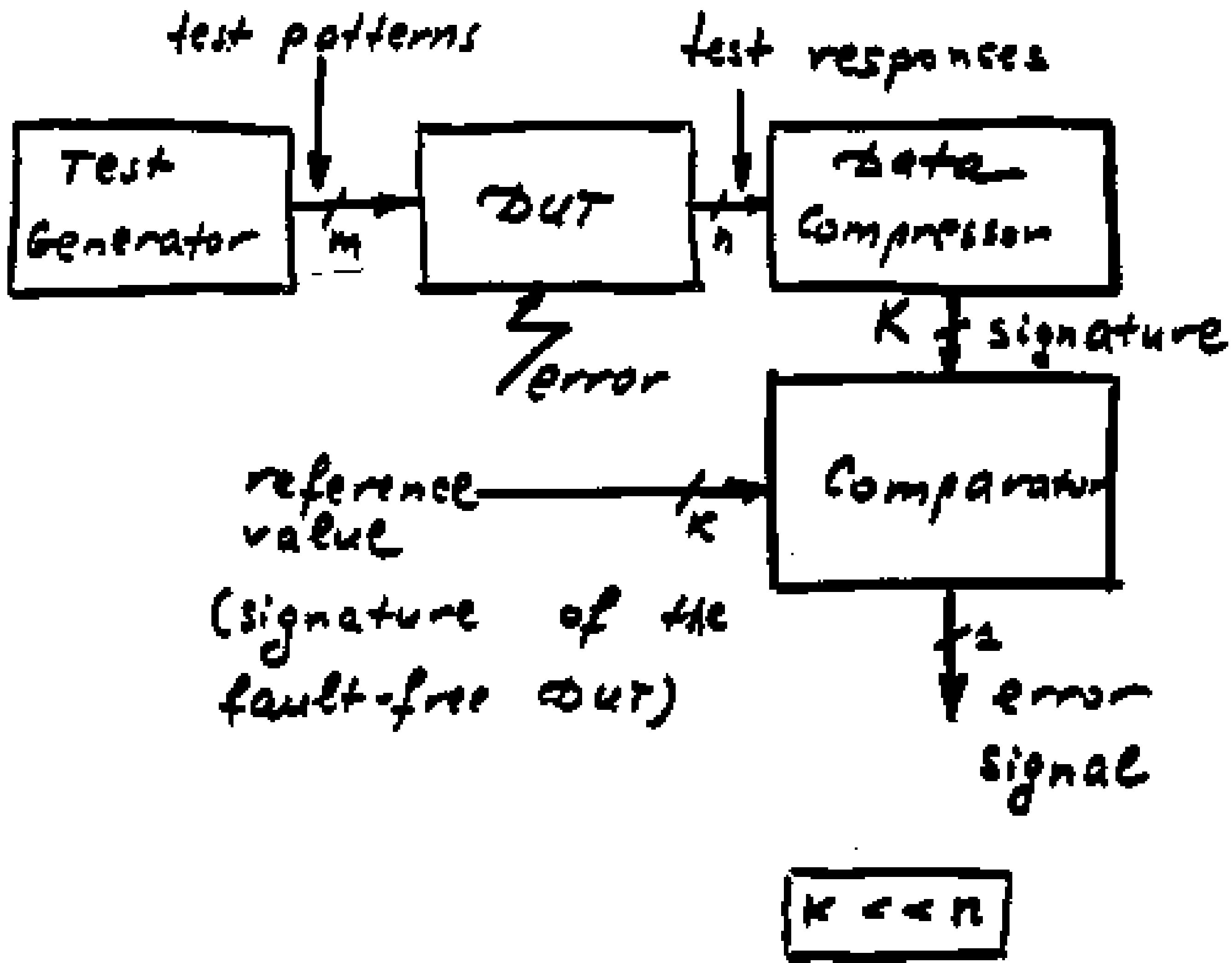
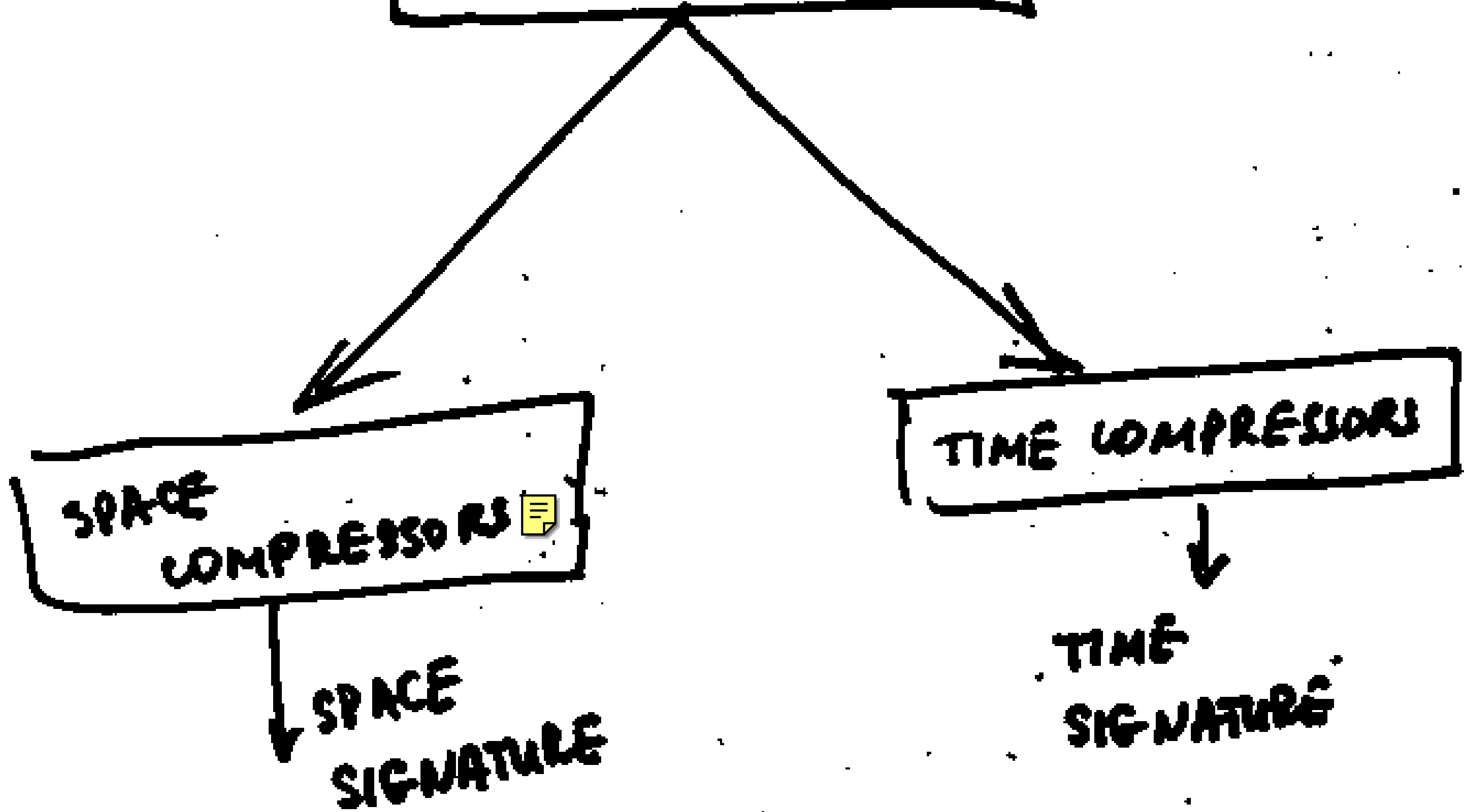
(1)

Data Compression of Test Responses

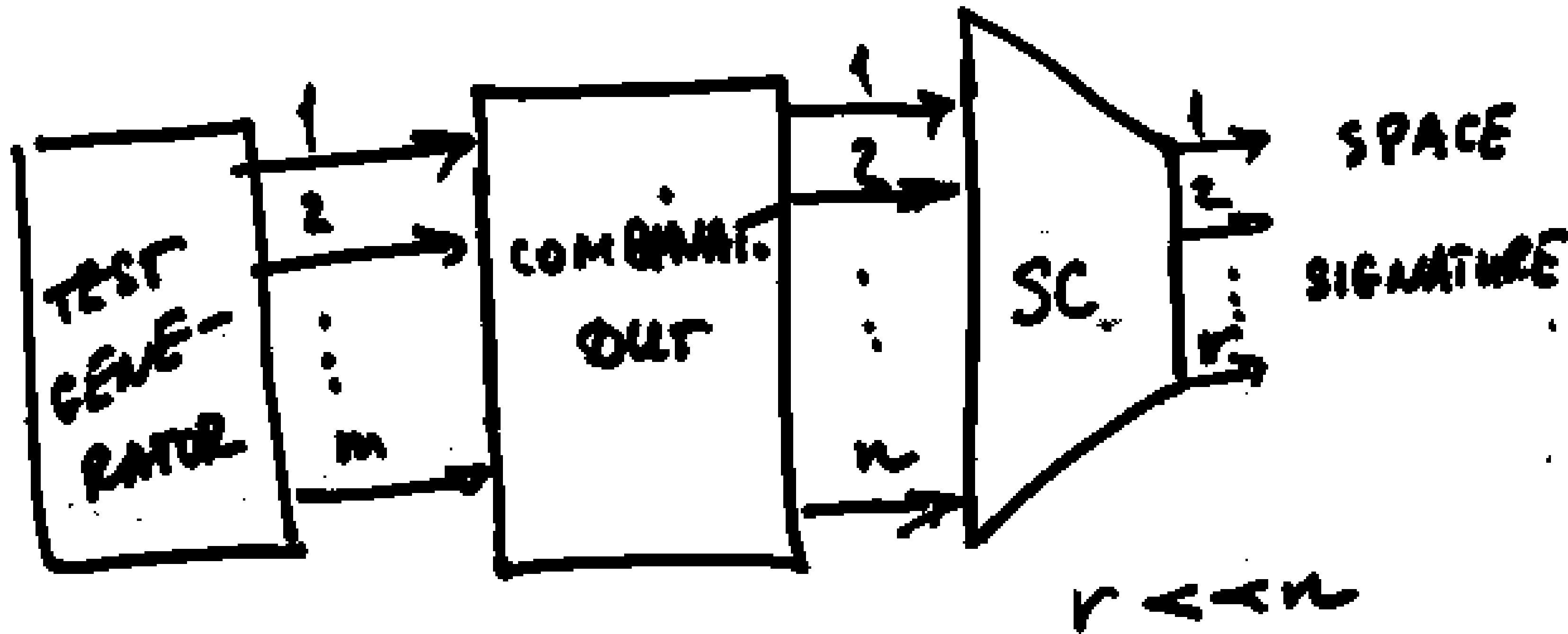
Time Compression

BIST




DATA COMPRESSORS
SPACE COMPRESSORS
TIME COMPRESSORS
SPACE SIGNATURE
TIME SIGNATURE

SPACE COMPRESSION



SC - space compressor
combinational device. based on
error CORRECTING CODES

E set of errors at the output of a DUT

$SC(y)$ - output of the SC,

y - output of a DUT

$e \in E$

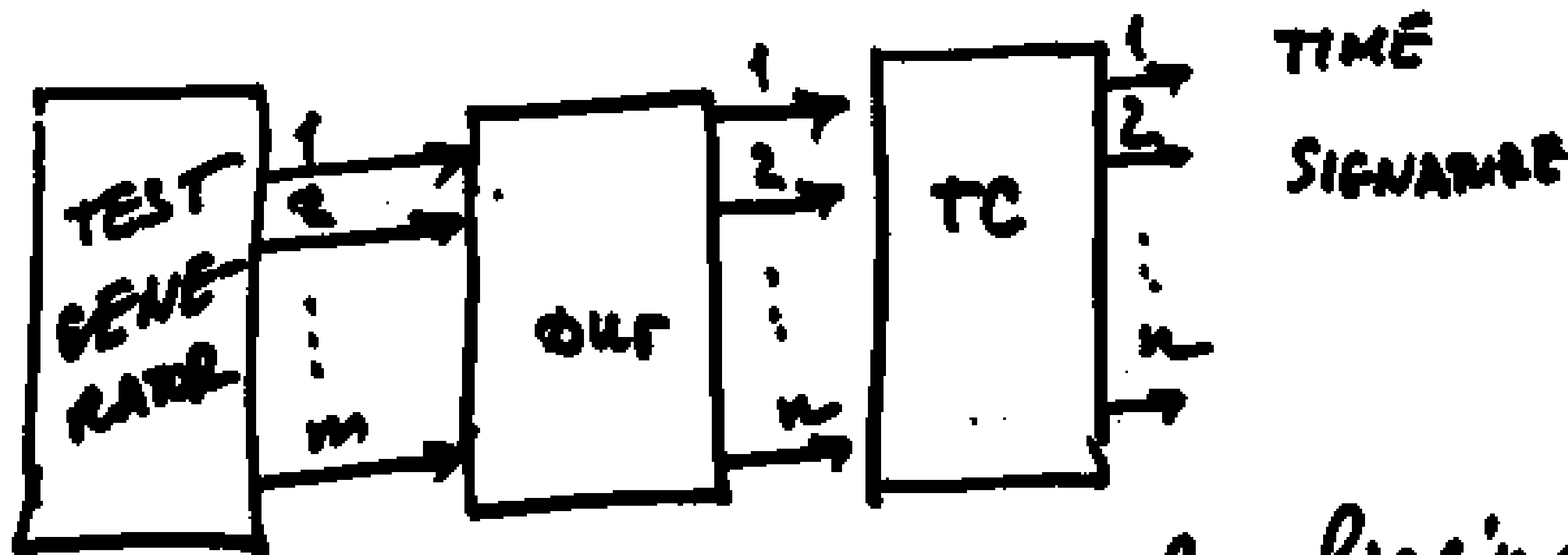
$y \Rightarrow y \oplus e$ SC - is a <u>combinational</u> device

$$SC(y) \neq SC(y \oplus e)$$

ERROR DETECTION BY MONITORING SC(y)

GOAL: $r \rightarrow min$

TIME COMPRESSION

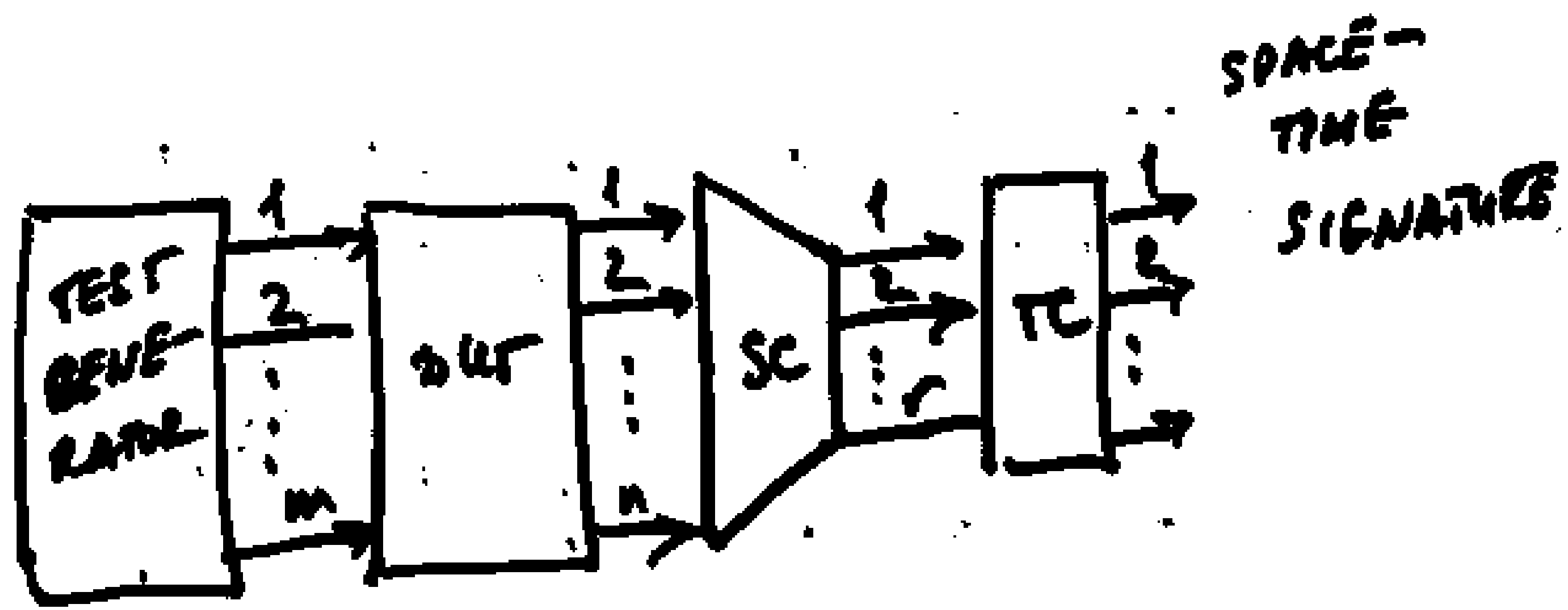


GOAL: MIN. P_{AL} – Prob of aliasing.:

$P_{AL} = Pr\{TC(y) = TC(y \oplus e)\}$ $e \in E$

TC – sequential device

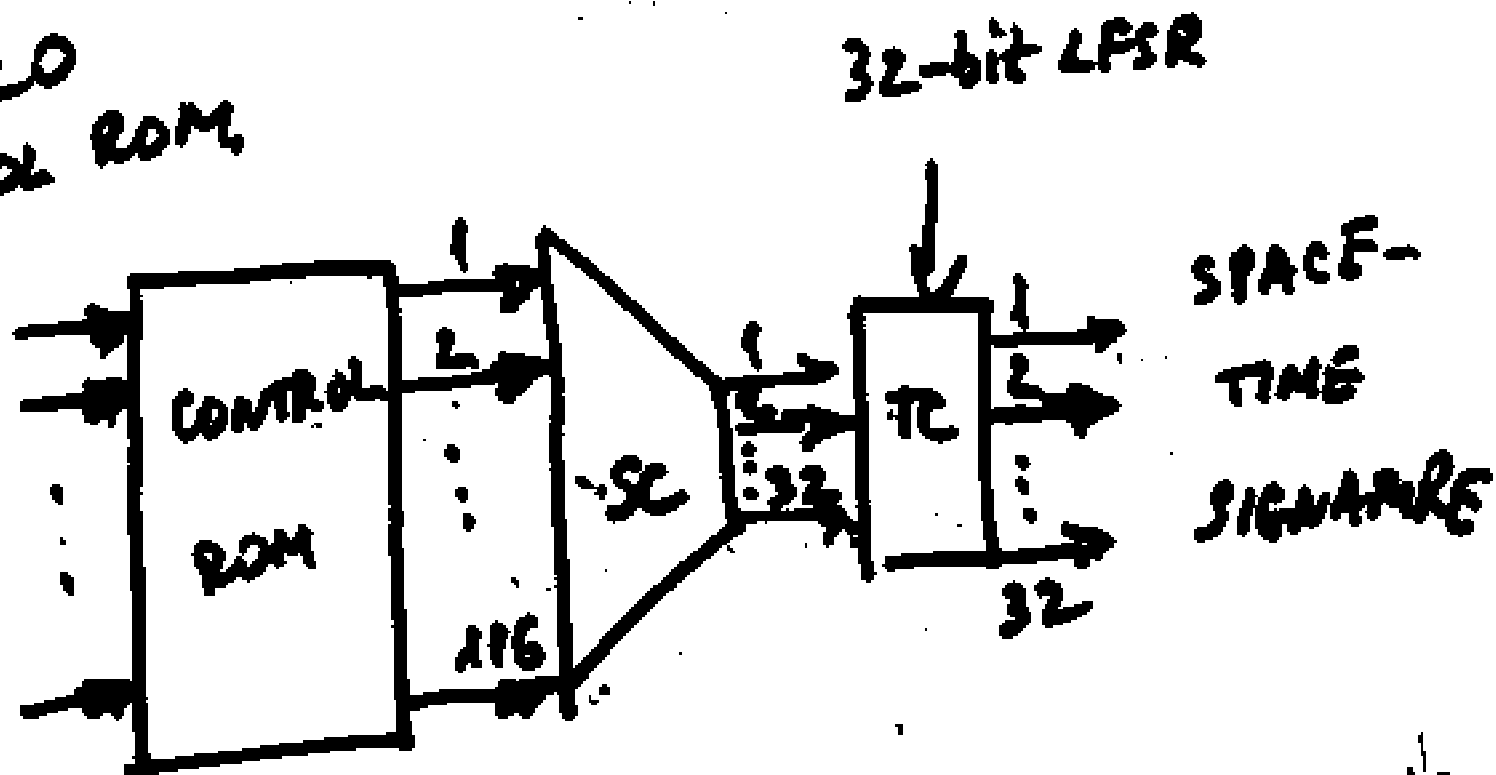
SPACE-TIME COMPRESSION



TRADEOFF
$$\begin{cases} r \to \min & \text{(overhead)} \\ P_{AL} \to \min \end{cases}$$

EXAMPLE

M68020 CONTROL ROM



Syndrome Testing

Data compression by addition

Exhaustive tests

Data compressor is an adder-accumulator

Normalized Syndrome

$$S_f = 2^{-m} \sum_{x} f(x)$$

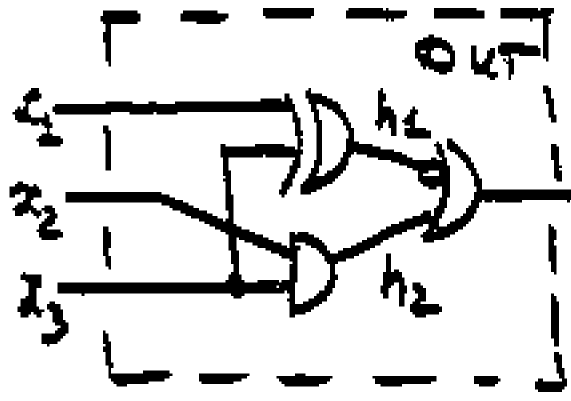
$x = (x_1, \ldots, x_m)$ - input vector

$f(x)$ - output of fault-free cut

with input $x = (x_1, \ldots, x_m)$

$$S_f = \text{Prob}\{f(x) = 1\}$$

Example ($m = 3$)



$y = f(x_1, x_2, x_3) = x_2 x_3 \vee \overline{x_1 \oplus x_3}$

x_1	x_2	x_3	f	$x_1/0$	$x_1/1$	$x_2/0$	$x_2/1$	$x_3/0$	$x_3/1$	$h_1/0$	$h_1/1$	$h_2/0$	$h_2/1$	$y/0$	$y/1$
0	0	0	1	1	0	1	1	1	0	1	0	1	1	0	1
0	0	1	0	0	1	0	1	1	0	1	0	0	1	0	1
0	1	0	1	1	0	1	1	1	1	1	0	1	1	0	1
0	1	1	1	1	1	0	1	1	1	1	1	0	1	0	1
1	0	0	0	1	0	0	0	0	1	1	0	0	1	0	1
1	0	1	1	0	1	1	1	0	1	1	0	1	1	0	1
1	1	0	0	1	0	0	0	0	1	1	0	0	1	0	1
1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1
S			5/8	6/8	0.5	0.5	5/8	0.5	6/8	1	2/8	0.5	1	0	1

All SSF's are detectable by syndrome testing S_f

Example $f(x_1, x_2, x_3) = \mathrm{maj}(x_1, x_2, x_3) =$

$= x_1 x_2 \vee x_1 x_3 \vee x_2 x_3 \Rightarrow S = 0.5$

If $x_i/0 \Rightarrow S = 0.25$

$x_i/1 \Rightarrow S = 0.75$

$f/0 \Rightarrow S = 0$, $f/1 \Rightarrow S = 1$.

Fault Coverages of Syndrome Tests

D1. A network is syndrome-testable if syndrome testing detects all SSF's

T.1. All fanout-free networks composed of AND, OR, NAND, NOR, NOT gates are syndrome-testable

D.2. A network is positive (negative) with respect to x_i if its output depends on x_i and does not depend on $\bar{x}_i$ (depends on $\bar{x}_i$ and do not depend on x_i)

D3. A network is unate if it is either positive or negative with respect to every input

Ex. $y = x_1 \oplus x_2$ non-unate

T2. All two-level AND-OR unate networks are syndrome testable

(J. Savir, IEEETC, C-49 pp 442-451, 1980)

+3 A two-level network can be made syndrome-testable for SSF's by the addition of one control line and at most one gate

(M. Miller, S. Eris, Electronic Letters, v.19, 16, 1983)

Syndrome testing is exhaustive

Optimal partitioning of CUT - NP-complete

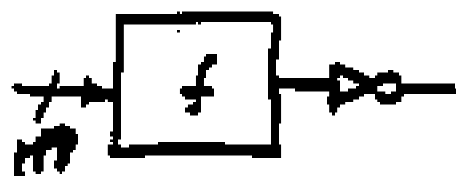
For multiple outputs networks:

separate adders for each output or

one parallel n-bit adder-accumulator

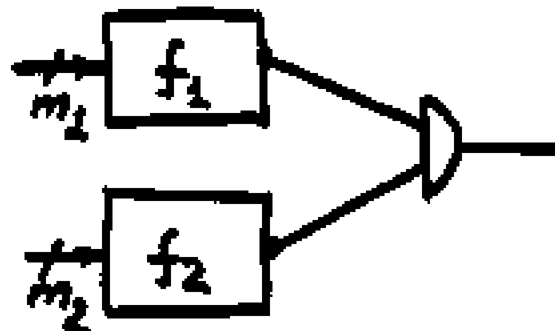
(n - is the number of outputs)

Computation of Syndromes

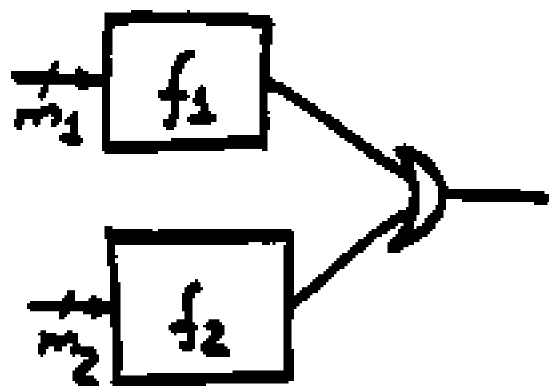


$1 - S_f$

For exhaustive tests

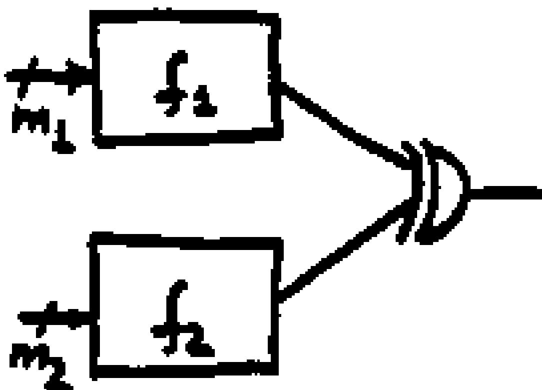


$S_{f_1} \cdot S_{f_2}$



$S_{f_1} + S_{f_2} - S_{f_1} \cdot S_{f_2}$

no fanouts at the inputs



$S_{f_1} + S_{f_2} - 2\, S_{f_1} \cdot S_{f_2}$

Syndrome Testing
(Summary)

Advantages:

1. SIMPLE DATA COMPRESSOR = adder - accumulator (small overhead)
2. Efficient for 2-level networks (for unate networks 100% of SSFs are detectable
3. Small overhead to make a two-level network syndrome testable
4. Computing reference values in a linear time.

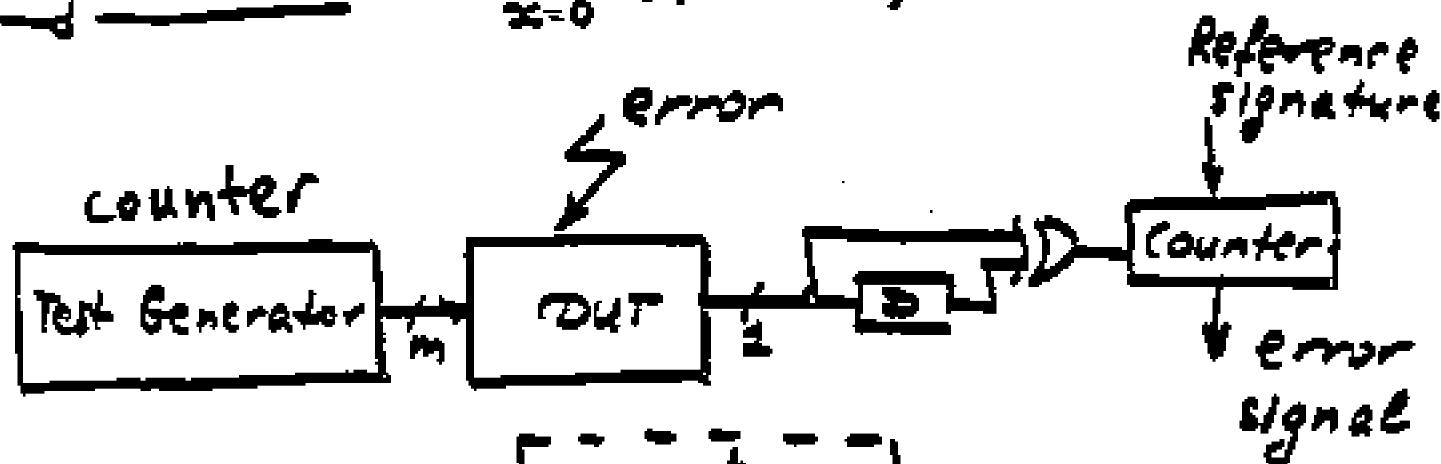
Disadvantages

1. Exhaustive testing for high fault coverage

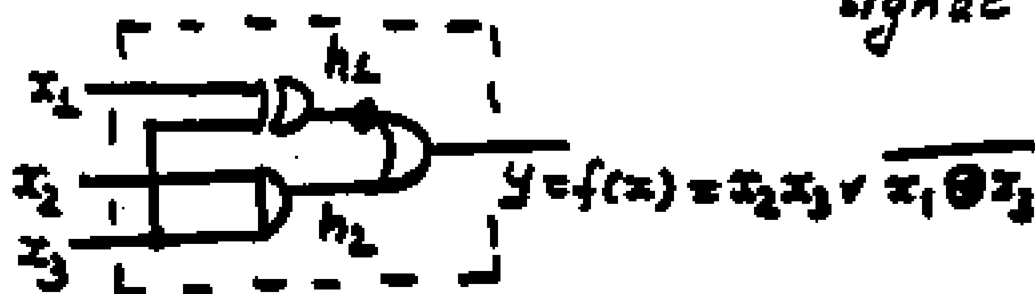
2. Partitioning problem (NP complete)

Transition Counting (TC)

Signature TC : $\sum_{x=0}^{2^m-1} \left(f(x) \oplus f(x+1) \right)$ — for exhaustive test.



Example $m=3$



$x_1\ x_2\ x_3$	f	$x_1/0$	$x_1/1$	$x_2/0$	$x_2/1$	$x_3/0$	$x_3/1$	$h_1/1$	$h_1/0$	$h_2/0$	$h_2/1$	$y/0$	$y/1$
0 0 0	1	1	0	1	1	1	0	1	0	1	1	0	1
0 0 1	0	0	1	0	1	1	0	1	0	0	1	0	1
0 1 0	1	1	0	1	1	1	1	1	0	1	1	0	1
0 1 1	1	1	1	0	1	1	1	1	1	0	1	0	1
1 0 0	0	1	0	0	0	0	1	1	0	0	1	0	1
1 0 1	1	0	1	1	1	0	1	1	0	1	1	0	1
1 1 0	0	1	0	0	0	0	1	1	0	0	1	0	1
1 1 1	1	1	1	1	1	0	1	1	1	1	1	0	1
TC	6	4	7	6	4	1	1	0	3	6	0	0	0

$x_2/0$ and $h_2/0$ cannot be detected by TC

For TC ordering in time of test patterns is essential.

Transition Counting

Optimal Ordering of Input patterns

T^0 set of test patterns producing 0

T^1 set of test patterns producing 1

$|T^0| \geq |T^1|$, $T = T^0 \cup T^1$, $|T| = |T^0| + |T^1|$

$AT = (t(1), t(2), t(3), \ldots)$ – Alternating test $\Rightarrow$ MAX TC.

$TC = |AT| - 1$

$t(1) \in T^0$, $t(2) \in T^1$, $t(3) \in T^0$, $t(4) \in T_1, \ldots$

length of a test may be greater than 2^n

T1 AT detects all SSF's by TC

[illegible] (this order maximizes TC for a fault-free device; faults decrease TC)

(J.P Hayes, IEEETC C-25, June 1976 pp 613-620)

T.1. is valid for any network consisting of AND, OR, NAND, NOR, NOT gates

FAULT-FREE ↳ $TC(f) > TC(\tilde{f})$ ← FAULTY for AT

f - fault-free

$\tilde{f}$ - faulty

$2|T| \geq |AT| \geq |T|$

$2 \cdot 2^m \geq |AT| \geq 2^m$ for exhaustive T

TC for AT is equal $|AT|$.

(9) (46)

Counting only $1 \to 0$ $(0 \to 1)$ transitions

Reddy, "A Note on Testing Logic Circuits by Transition Counting" IEEE TC ~~EC-25~~, March 1977 pp 313-314. **FOR UNIDIRECTIONAL ERRORS**

transition Counting for sequential devices (without **LSSD**)

"Transition Count Testing for Sequential Machines" Proc. Int. Symp on Fault-Tolerant Computing, Japan Oct. 1980, pp 167-172

Fault-Location by Transition Counting – very difficult

For n input NAND gate:

$$\frac{n^2}{8}+1 \le T(n) \le \frac{n(n+1)}{2} + 2$$

(For detection $T(n) = n+1$)

Hayes, "Testing by Transition Counting", Int. Symp on Fault-Tolerant Computing", June 1975 pp 215-222