DIAGNOSTIC TESTING

GOAL: IDENTIFY FAULTY COMPONENTS

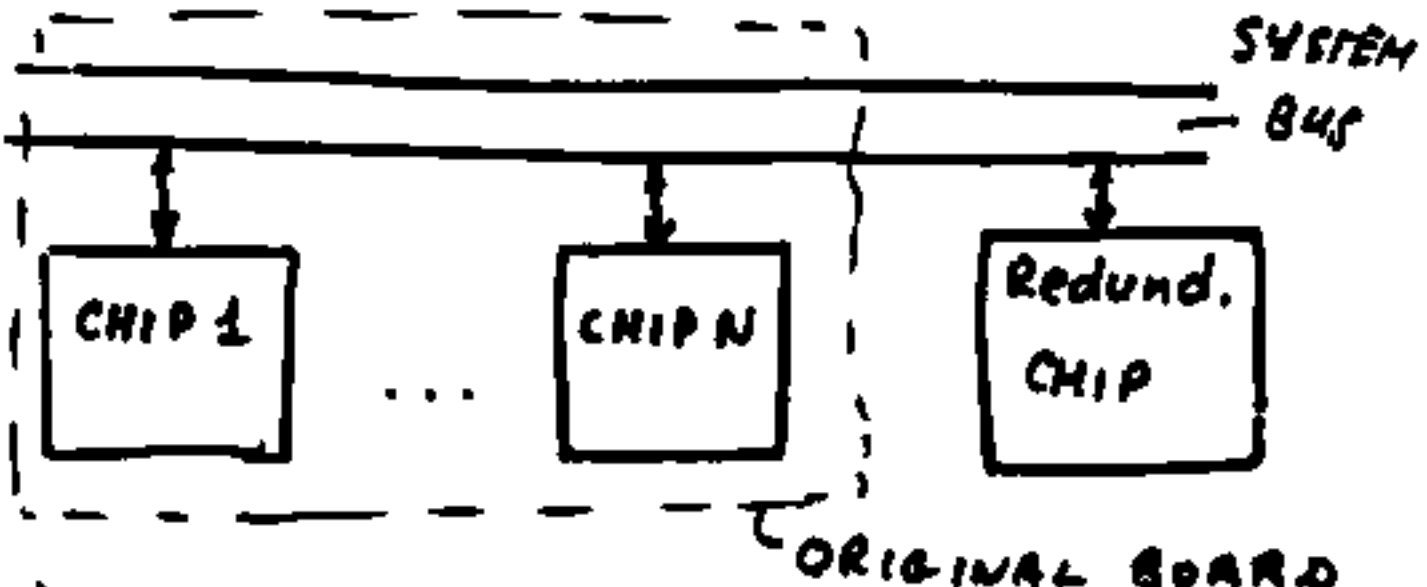
(FAULTY CHIP ON BOARD,
FAULTY BOARD IN A SYSTEM)

APPROACH: ADD AN ADDITIONAL COMPONENT WHICH WILL ANALYZE RESPONSES OF ALL COMPONENTS IN THE ORIGINAL SYSTEM AND IDENTIFY FAULTY COMPONENTS.

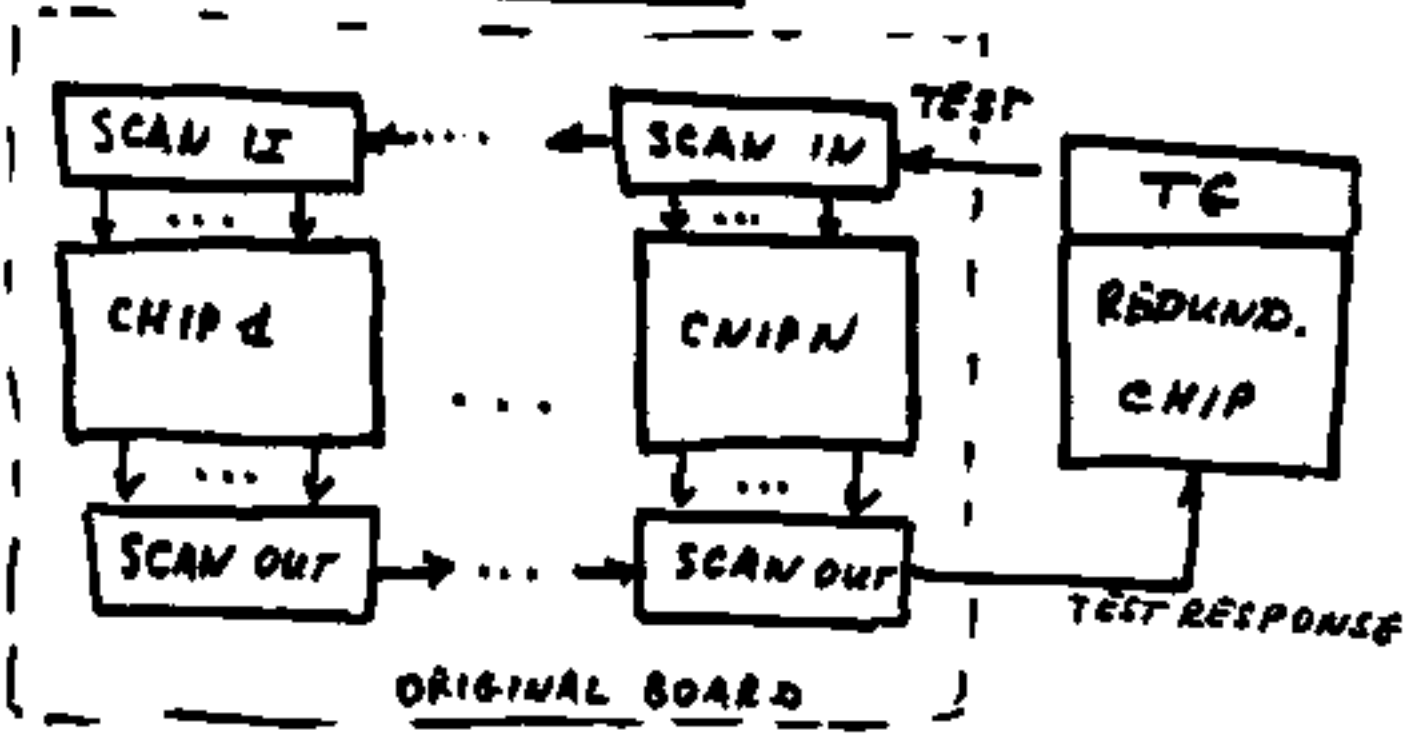
IDENTIFICATION OF A FAULTY CHIP ON BOARD

IN THE TESTING MODE.

1) WITH SYSTEM BUS:



2) WITH BOUNDARY SCAN:



FUNCTIONS OF THE REDUNDAND CHIP:

1. GENERATE A TEST (e.g. BY LFSR)
2. ANALYZE RESPONSES OF ALL THE CHIPS ON THE ORIGINAL BOARD AND IDENTIFY FAULTY CHIPS

Approaches for Board-Level-Diagnostic

1. STRAIGHTFORWARD APPROACH (TESTING EACH CHIP SEPARATELY!
2. SPACE-TIME COMPRESSION APPROACH

1. STRAIGHT FORWARD APPROACH FOR DIAGNOSTIC

FOR A BOARD WITH N CHIPS REDUND. CHIP CONTAINS:

1. LFSR FOR TEST GENERATION
2. N LFSRs FOR COMPRESSION RESPONSES FROM CHIPS
3. N memory cells to store REFERENCE VALUES FOR DIFFERENT CHIPS
4. N MATCH DETECTORS
5. CONTROLLER.

∴ STRAIGHTFORWARD APPROACH PROVIDES FOR MULTIPLE FAULTY CHIP ERROR-LOCATING-CAPABILITY BUT IT REQUIRES CONSIDERABLE HARDWARE OVERHEAD.

∴ SPACE-TIME APPROACH PROVIDES FOR SINGLE FAULTY CHIP ERROR-LOCATING-CAPABILITY BUT REQUIRES SMALL OVER-HEAD

BOARD - LEVEL DIAGNOSTICS BY SPACE-TIME COMPRESSION

1. SPACE COMPRESSION

Let $Z_0(t), Z_1(t), \ldots, Z_{N-1}(t)$ - TEST RESPONSES OF THE CHIPS ON BOARD AT THE MOMENT t

where $Z_i(t)$ is AN M-bit binary vector

and $N < 2^M$

COMPUTE TWO SPACE Signatures:

$$y(t) = Z_0(t) + Z_1(t) + Z_2(t) + \ldots + Z_{N-1}(t)$$

$$y^*(t) = Z_0(t) + x Z_1(t) + x^2 Z_2(t) + \ldots + x^{N-1} Z_{N-1}(t)$$

M.G. KARPOVSKY, P. NAGVAJARA
"DESIGN OF SELF-DIAGNOSTIC BOARDS BY SIGNATURE ANALYSIS", IEEE TRANS ON INDUSTRIAL ELECTRONICS, MAY 1989

M.G. KARPOVSKY, P. NAGVAJARA
"BOARD-LEVEL DIAGNOSIS BY SIGNATURE ANALYSIS" PROC. IEEE Int. TEST CONF, 1988 pp 47-53

2. Time Compression

Sequences of space signatures

$(y(0), y(1), \ldots, y(T-1))$ and

$(y^*(0), y^*(1), \ldots, y^*(T-1))$ are compressed

in time by two identical LFSRs,

where T is a number of test patterns

Let $(\bar{S}, \bar{S}^*)$ are the resulting time

signatures and (S, S^*) the corresponding reference values.

$$\Delta S = \bar{S} + S$$
$$\Delta S^* = \bar{S}^* + S^*$$

$\Rightarrow$ distortions of time signatures

Identification of a faulty chip

CHIP NUMBER i IS FAULTY IFF:

$$\Delta S^* = x^i \Delta S \qquad i \in \{0,1,\ldots,N-1\}$$

IF $\Delta S \neq \overbrace{(0,\ldots,0)}^{M}$ OR $\Delta S^* \neq \overbrace{(0\ldots,0)}^{M}$

AND $\Delta S^* \neq x^i \Delta S$ FOR ALL $i=0,1,\ldots,N-1$,

THEN THERE ARE AT MOST TWO FAULTY CHIPS ON BOARD.

EXAMPLE 1

$M = 3$ outputs per chip

$N = 5$ chips on the board

TAKE $P(x) = x^3 + x + 1$ (PRIMITIVE FOR LFSRs)

t	BINARY	POLYNOMIAL	EXPONENTS
0	0 0 0	0	
1	0 0 1	1	x^0
2	0 1 0	x	x^1
3	0 1 1	$x+1$	x^3
4	1 0 0	x^2	x^2
5	1 0 1	x^2+1	x^6
6	1 1 0	x^2+x	x^4
7	1 1 1	x^2+x+1	x^5

SUPPOSE THAT CHIP #4 is FAULTY

AND $Z_4(1)$ and $Z_4(5)$

are distorted

$Z_4(1) : 011 \longmapsto 110$

$Z_4(5) : 101 \longmapsto 010$

$$g(x) = c_2 x^2 \oplus c_1 x \oplus c_0 \quad , c_i \in \{0,1\}$$

x^2	x	1	exp	mod $p(x)$	log
0	0	0	0		-
0	0	1	x^0		0
0	1	0	x^1		1
0	1	1	x^3		3
1	0	0	x^2		2
1	0	1	x^6		6
1	1	0	x^4		4
1	1	1	x^5		5

$x^2 \oplus x \oplus 1$

$7 = 2^3 - 1$ ← b

$x^3 \oplus x^2 \oplus x \oplus 1$ — not primit

$x^7 = x^3 \oplus x = 1 = x^0$

$x^6 = x^3 \oplus x^2 \oplus x = x^2 \oplus 1$

$x^5 = x^3 \oplus x^2 = x^2 \oplus x \oplus 1$

$x^4 = x^2 \oplus x$

$x^3 = x \oplus 1$ — PRIMITIVE

$x^3 \oplus x \oplus 1 = p(x) = 0$

EXAMPLE 1 (CONT'D)

THEN

$\Delta Z_4(1) = e_4(1) = 101 = x^6$ error

$\Delta Z_4(5) = e_4(5) = 111 = x^5$ function

FOR ALL OTHER $\begin{matrix} i \\ t \end{matrix}$: $\Delta Z_i(t) = 0$

distortions in space SIGNATURES

$\Delta y(1) = x^6$, $\Delta y^*(1) = x^6 \cdot x^4 = x^{10} = x^3$

$\Delta y(5) = x^5$, $\Delta y^*(5) = x^5 \cdot x^4 = x^9 = x^2$

$x^i \cdot x^j = x^{i+j \pmod 7}$

SINCE $y(t) = \sum_{i=0}^{N-1} Z_i(t)$, $y^*(t) = \sum_{i=0}^{N-1} x^i Z_i(t)$

T FLIP-FLOPS / LFSR 1.

EXAMPLE 2 (CONT'D)

DISTORTIONS IN TIME SIGNATURES

$$\tilde{S}=\tilde{S}(T)= x(\ldots x(x(x\tilde{y}(0)+\tilde{y}(1))+\tilde{y}(2))\ldots\tilde{y}(T-2)$$

$$+\tilde{y}(T-1)=$$

$$= x^{T-1}\tilde{y}(0)+x^{T-2}\tilde{y}(1)+\ldots+x\tilde{y}(T-2)+$$

$$+\tilde{y}(T-1)=\sum_{i=0}^{T-1} x^{T-i-1}\tilde{y}(i)$$

T - IS A NUMBER OF TEST PATTERNS

AND

$$\tilde{S}^*=\tilde{S}^*(T)=\sum_{i=0}^{T-1} x^{T-i-1}\tilde{y}^*(i) \qquad T=7$$

THUS

$$\Delta\tilde{S}=S+\tilde{S}=\sum_{i=0}^{T-1} x^{T-i-1}\Delta y(i)$$

$$\Delta\tilde{S}= x^{T-1}x^0+x^{T-6}\,x^5=x^{T-1}(x^5+1)$$

$$\Delta\tilde{S}^*=S^*+\tilde{S}^*=\sum_{i=0}^{T-1} x^{T-i-1}\Delta y^*(i)$$

$$\Delta\tilde{S}^*=x^{T-2}\cdot x^3+x^{T-6}x^2=x^{T-4}(x^5+x^{-3})$$

$$=x^{T-4}(x^2+x^4)$$

SINCE $x^{-3}=x^4$ $\quad(x^3\cdot x^4=x^7=1)$

EXAMPLE 1 (CONTD)

Identification of a faulty chip

NOTE THAT

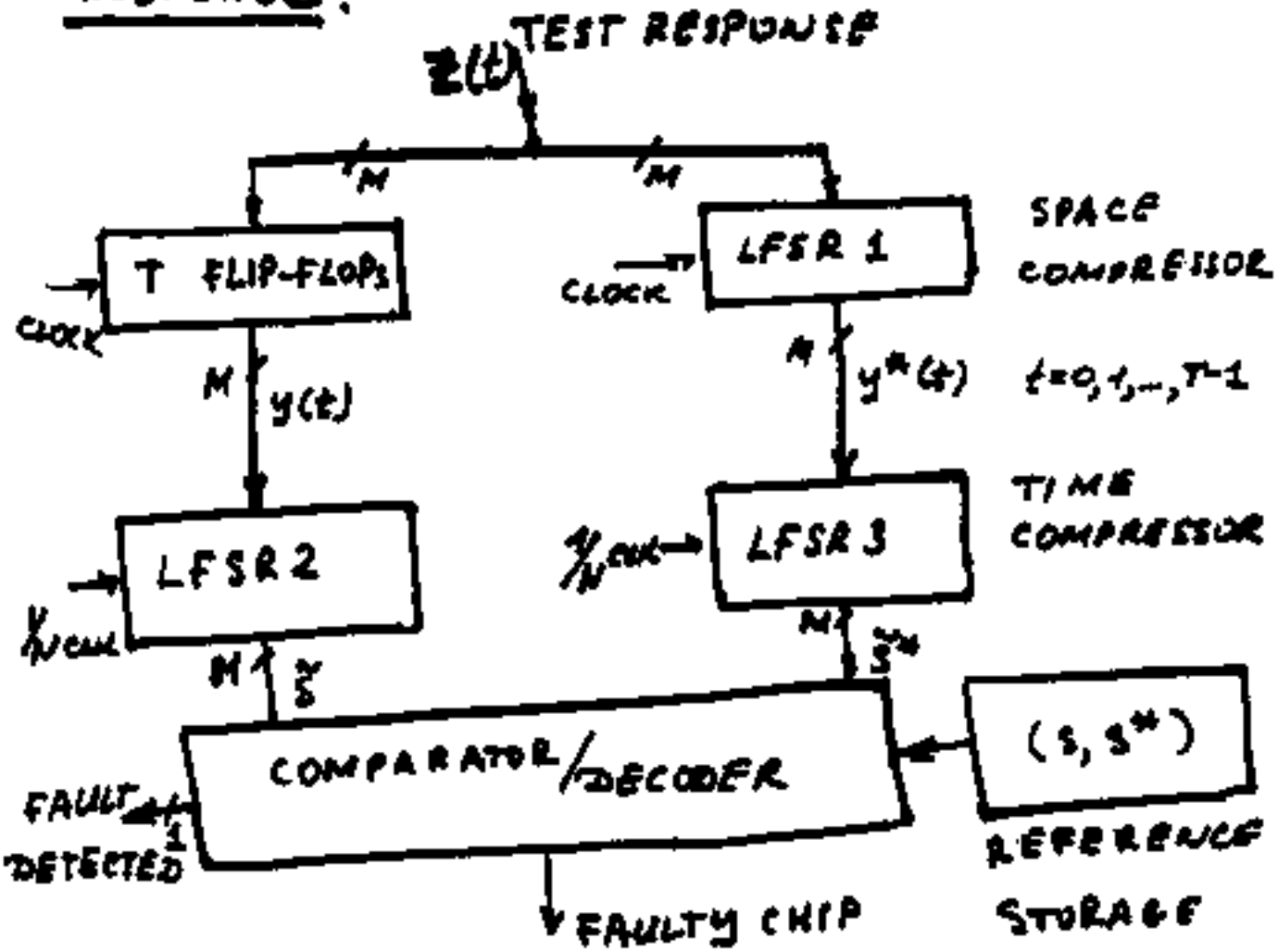
$$\Delta\tilde{S}\cdot x^4 = x^{T-1}(x^5+1)\,x^4 = x^T(x^9+x^4) =$$

$$= x^{T-1}(x^2+x^4) = \Delta\tilde{S}^4$$

($\Delta\tilde{S}\cdot x^i \neq \Delta\tilde{S}^4$ FOR $i\neq 4$)

THUS: CHIP #4 IS FAULTY.

HARDWARE IMPLEMENTATION OF BOARD-LEVEL DIAGNOSTICS BY SPACE-TIME COMPRESSION OF TEST RESPONSES.

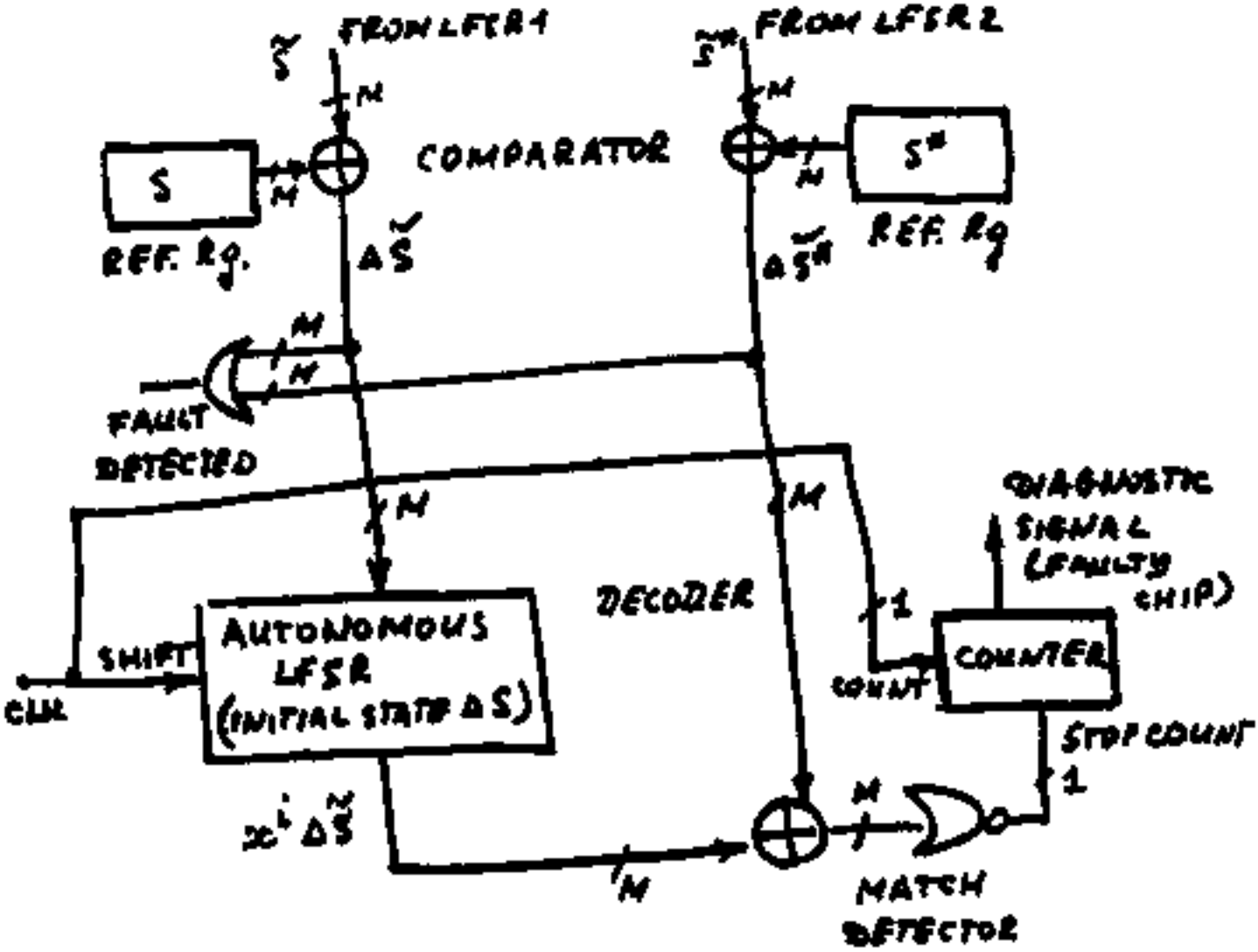


LFSR 1 = LFSR 2 = LFSR 3

DECODING AND IDENTIFICATION OF A FAULTY CHIP

CHIP i IS FAULTY IFF :

$$\Delta \tilde{S}^* \triangleq \tilde{S}^* + S^* = x^i \Delta \tilde{S} = x^i (\tilde{S} + S)$$



If $\Delta \tilde{S}^* \neq x^i \Delta \tilde{S}$ FOR ALL $i = 0, 1, \ldots, N-1$

AND ΔS^* or $\Delta S \neq 0$ THEN THERE ARE AT <u>LEAST TWO</u> FAULTY CHIPS

COMPARISON BETWEEN STRAIGHTFORWARD DIAGNOSTICS AND SPACE-TIME DIAGNOSTICS

OVERHEAD ANALYSIS

NUMBERS OF EQUIVALENT TWO-INPUT GATES

M=16 (16 output pins for every chip)

Approach \ NUMBER OF CHIPS ON BOARD N	8	16	24	32	64
STRAIGHT-FORWARD	1,931	3,579	5,355	7,059	13,939
SPACE-TIME DIAGNOSTICS	1,714	1,726	1,738	1,748	1762

SAVINGS IN GATE COUNTS

M=16 bits in output of every chip

N - chips on BOARD

N	8	16	24	32	64
P	11%	52%	68%	75%	87%

∴ SPACE-TIME DIAGNOSTICS PROVIDES FOR CONSIDERABLE SAVINGS IN OVERHEADS BUT CAN IDENTIFY ONLY SINGLE-FAULTY-CHIP ERRORS

∴ PROB. OF MASKING SINGLE-CHIP FAULT 2^{-M} AND MULTIPLE-CHIP-FAULTS AT MOST 2^{-2M}